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Design and Control of Single-Phase Modified Multilevel Converter for Photovoltaic Applications

by:

Majdi Thaher

Supervisors:

Dr. Hakam Shehadeh & **Dr. Jamal Siam**

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Design and Control of Single-Phase Modified Multilevel Converter for Photovoltaic Applications

التَصمِيمُ والتَحكمُ في مُحول مُتعددِ المُستَويات مُعدل أُحادي الطَور للتطبيقَاتِ الكَهروضَوئية

by:

Majdi Thaher

Approved by the Examining Committee

Supervisors:

Dr. Hakam Shehadeh ....

Dr. Jamal Siam ....

Examiners:

Dr. Muhammad Abu-Khaizaran ....

Dr. Jaser Sa'ed ....

Birzeit, Palestine

June 23rd, 2021

Declaration of Authorship

I declare that this thesis titled, "Design and Control of Single-Phase Modified Multilevel Converter for Photovoltaic Applications" and the work presented in it is my own. I confirm that:

- This work was done wholly or mainly while in candidature for a Master degree at Birzeit University.

- Where any part of this thesis has previously been submitted for a degree or any other qualification at this University or any other institution, this has been clearly stated.

- Where I have consulted the published work of others, this is always clearly attributed.

- Where I have quoted from the work of others, the source is always given. With the exception of such quotations, this thesis is entirely my own work.

- I have acknowledged all main sources of help.

- Where the thesis is based on work done by myself jointly with others, I have made clear exactly what was done by others and what we have contributed myself.

Signed:

Majdi Thaher

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Date:

June 23rd, 2021

المستخلص

تقترح هذه الرسالة عاكس مهجن للطاقة الكهربائية متعدد المستويات أحادي الطور ذي الوحدات المركبة، والذي يسمى دارة الخلايا المضافة المركبة (MAC) ، والتي يمكن استخدامه في مجموعة متنوعة من تطبيقات أنظمة الطاقة. يحتوي التركيب المقترح على عدد أقل من مصادر الطاقة ومفاتيح التبديل الفعالة وغير الفعالة لكل مستوى فيما يتعلق بالعديد من المكونات الموجودة. كما أن لديه القابلية لرفع عدد المستويات من خلال التطوير الهيكلي وتضخيم اشارة الجهد بنسب مختلفة. هنا طبق العاكس من نظام تيار ثابت الى تيار متردد، يتم تقديم مقارنة بين MAC وعدة عواكس اخرى تقليدية وحديثة لتوضيح ميزاتها التنافسية. يتكون MAC من ثلاث وحدات رئيسية: الأولى ألفا (α) المسؤولة عن توليد مستويات الجهد الإيجابي المطلوبة لنصف الدورة الموجبة كنموذج أساسي ، الثانية بيتا (β) وهي خلية مضافة تحدد إجمالي عدد مستويات الجهد الناتج في حالة النموذج الموسع من MAC ولها ثلاثة تصاميم، والوحدة الأخيرة جاما (γ) التي تعكس الجهد لتوليد مستويات نصف الدورة السلبي. يستخدم تطبيق عاكس مختلف النماذج لـ MAC متعدد المستويات المتوسط لتوضيح حالات التشغيل ، ومفاتيح التبديل الفعالة ، ومسارات الإشارة لكل مستوى تبديل. أخيرًا ، يتم التحقق من صحة عمل تصميم عدة نماذج مشتقة من MAC عن طريق محاكاة عاكس MAC لعدة مستويات مختلفة، مع نوعين من الربط الكهربائي: الاول منفرد بنظام تحكم مبني على تقنية عرض النبضة الجيبية بعدة مصادر (SPWM)، وبنموذج التحكم التنبؤي ذو اوضاع التحكم المحدد باستخدام مصدر واحد (FCS-MPC) وهذا النموذج يطبق ايضا في النوع الثاني عند الربط بالشبكة الكهربائية باستخدام مصدر واحد، بالاضافة الى دراسة شكل اشارات الجهد والتيار ونسبة التشوه في كل حالة بناء على عدد من المعايير منها: عدد المستويات، عدد المكونات في كل نموذج مشتق من العاكس، تضخيم الجهد، ... الخ. تم في هذه الرسالة تقديم التصميم النظري للعاكس، تحليل النموذج الرياضي لهذه الدارة، وعبر برنامج الحاسوب: MATLAB / SIMULINK تم عرض نتائج المحاكاة الهندسية لهذه الدارة ومشتقاتها. بناء على هذه النتائج حقق العاكس بتوليد اكبر عدد من المستويات عند اقل عدد من المفاتيح والمصادر الكهربائية بالمقارنة بالعواكس الاخرى.

Abstract

This thesis proposes a single-phase hybrid modular multilevel power-converter topology, called Modular Added Cell (MAC), which can be used in a variety of power energy applications. The proposed topology has a reduced number of sources and active switches per level with respect to several existing ones. It also has voltage boosting and structural-scalability. Here, MAC is applied for inverter (DC to ac system). A comparison of MAC to several other topologies is introduced to illustrate its competitive features. The MAC topology is composed of three main modules: the first, α, generates the required positive-cycle voltage levels, the second, β with three different types, reverses the voltage to generate the negative-cycle levels. The last module, γ, is a modular added cell that defines the total number of output voltage levels. The analysis of averaged multi-level MAC converter then used to illustrate the operation states, active switches, and signal paths for each switching level. Finally, the MAC topology operation is validated by the simulation of different forms of MAC inverter in two connections; the first one is standalone connection with two different control methods based on: Sinusoidal Pulse Width modulation (SPWM) for multiple DC-Source configuration and Finite Control Set -Model Predictive Control (FCS-MPC) for single DC-Source. The second is Grid-connected which is also applied using previous FCS-MPC in single DC-source configuration. several parameters were studied such as: number of voltage levels, components count, voltage gain, …etc. The theoretical design and analysis, mathematical model of MAC, and simulation results are presented by MATLAB/SIMULINK. The proposed MAC topology has reduced switches and sources count with big number of voltage levels verses other topologies.

Contents

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List of Symbols and Abbreviations

1-DCS	Single **DC-S**ource ratio configuration
FCS-MPC	**F**inite **C**ontrol **S**et-**M**odel **P**redictive **C**ontrol
LS-SPWM	**L**evel **S**hift **-** **S**inusoidal **P**ulse **W**idth **M**odulation
MAC	**M**odular **A**dded **C**ell
MAC7 (1-DCS)	**7**-Level **M**odular **A**dded **C**ell Converter using single DC-source
MAC11-β1 (1-DCS)	**11**-Level Extended-**MAC** Converter using single **B**eta-1 cell
MAC49-2αc	**49**-Level **MAC** Converter using double cascaded **Alpha** Modules
M-DCS	**M**ultiple **DC**-Source ratio configuration
MLC	**M**ultilevel **C**onverter
MLI	**M**ultilevel **I**nverter
MMC	**M**odular **M**ultilevel **C**onverter
N	Number of Added Cells (Beta-cells)
N$_α$	Number of alpha modules
N$_C$	Number of total capacitors
N$_D$	Number of total diodes
N$_L$	Number of voltage levels
N$_S$	Number of total sources
N$_{SW}$	Number of total switches
RCC	**R**educed **C**omponent **C**ount Strategy
SC	**S**witched-**C**apacitor **T**opology
SM	**S**ub **M**odule
THD	**T**otal **H**armonic **D**istortion
V$_{main}$	The **Main Voltage-reference source** and has the biggest value
V$_{sec}$	The **secondary Voltage-reference**, it's a source in 1-DCS and a capacitor in M-DCS
xMAC	**E**xtended-**MAC** Topology
xMAC-α	**x**MAC Converter based on **A**lpha modules
xMAC-β	**x**MAC Converter based on **B**eta cells

CHAPTER 1
INTRODUCTION

In the Last decennium of this century, solar photovoltaic (PV) and electric vehicles (EV) were highly expected to play an important role in the electric industry in the next decades.

These technologies, and other renewable energy resources, have been worth concern the optimal solution for researchers, academics, and industries due to:

- The increase of carbon dioxide (CO_2) emission and its harmful environmental impacts caused by power oil generation stations and traditional vehicles.

- The need of new clean electric power sources, and to compensate the limitations of the fuel quantities and high pricing effects.

Power converters have been designed to ease the integration of different power resources systems into the distribution grid or to use standalone [1]-[3]. Multilevel converter (MLC) is one of the most attractive converter topologies for several power applications. This converter has the important features of enhanced power quality with lower harmonic distortion, lower rate of change of voltage (dv/dt), and the capability to handle high power with low switching frequency [4]. The output power quality is usually improved by increasing the number of output voltage levels; however, this leads to increase the number of power switches and gate driver circuits, size, cost, and control complexity [5]. This makes developing new converter topologies that improves the output power quality with reduced converter structural and control complexities an important research concern in the field of microgrids and other electric power systems.

1.1 Problem Statement & Motivations

Developing a multilevel converter topology involves satisfying a set of possibly contradicting constraints, among these are:

- o Number of components

- o Number of main DC voltage sources

- o Number of active switches at each state of operation and output voltage level.

- o Topology modularity and scalability, which means the possibility extending the structure by adding specific modules to obtain new converters with higher number of output levels.

- o Output voltage gain boosting ability for output. This study proposes a converter topology called Modular Added Cell (MAC) that aims to reduce the number of the converter's electronic switches, number of employed DC voltage sources, number of active switches per operation state, and improved output voltage boosting capability,

- o Grid-connected/Standalone operation modes and control schemes.

1.2 Contribution

The study main contributions are:

Development of modified hybrid multilevel inverter topology with:

- • Dual and Single DC main-supply 9-levels basic topology.

- • Voltage levels number scalability using ad-hoc modular added cells extension topology.

- Enhanced number of electronic switches for specific voltage levels.

- Enhanced voltage boosting-gain capability.

- Enhanced number of active switches for several operation states and voltage-levels.

- Grid-connected and Standalone operation modes.

- Possibility of employment as inverter.

1.3 Research Goals

The rest of objectives of this thesis are as follows:

- Design a multilevel converter topology based on simplified half and full bridge modules to achieve reduced components count structure; maximum voltage level with minimum power, components, and DC sources. This topology includes different scalable added cells to have more option with several features.

- To improve total harmonics distortion ratio (THD)

- To examine the proposed converter for several developed hybrid MAC schemes for two configurations; single source and multiple DC-sources.

- To apply capacitor voltage balancing technique on the proposed converter for different levels number (nine, seven, and eleven levels) of single source multilevel inverters in basic and extended forms, this part is applied in single DC-source configuration. Also, this is examined for closed loop grid-connected case, and for the nine-level inverter in standalone case.

- In multiple DC-sources configuration, the voltage-references are DC-sources, and the case is applied in open-loop Standalone.

- Simulation based validation via MATLAB/SIMULINK software.

1.4 Thesis Organization

The rest of this thesis is organized as follows:

- Chapter 2 includes a literature review of multilevel inverters (MLI) and their applications in renewable energy applications and electric vehicles. This chapter also summarizes the advantages and disadvantages of the most competitive known topologies with special focus on the number of employed electronic switches.

- Chapter 3 presents the proposed modified converter structure, modular added cells structures, and structure extension schemes. It also illustrates the possibility of employment of the proposed topology as an MMC and its operation features.

- Chapter 4 describes the MAC basic principle of the operation, parameters calculations as number of levels, voltage-boosting gain, and other features.

- Chapter 5 illustrates the different topologies of MAC inverter. In addition, it illustrates the operation and control of single-phase MAC inverter with inductive load settings.

- Chapter 6 presents the simulation results of the system using MATLAB/SIMULINK.

- Chapter 7 includes discussion and conclusion.

CHAPTER 2
LITERATURE REVIEW

This chapter reviews the most-known inverter topologies, their structure, advantages, disadvantages, and other limitations.

2.1 Multilevel Converter

Multilevel inverter (MLI) is one of the most suitable solutions to enhance the performance of renewable energy systems such as photovoltaic (PV) energy systems, electric vehicles (EV's), and other power electronics application in power systems [6]. MLI generates stair-case voltage levels, which approximate a sinusoidal electric signal. The structure and the number of levels of this type of converter set the accuracy of the approximated signal and provide the converter with several beneficial features such as the capability to handle high voltage with reduced switching and conduction losses, enhanced power quality by decreasing the total harmonics distortion (THD) and lower switching frequency [7].

2.2 Classification of Multilevel Topologies

Several MLI topologies were developed in recent years to achieve the best approximation and performance in terms of power losses and harmonic distortion. One of the most important features of this type of topology is the design the DC main sources from which the different levels are obtained. Several existing topologies employed symmetric voltage sources; whereas, others used asymmetric sources with the objective of achieving higher number of voltage levels with a lower number of components. Existing MLI topologies were also classified

according to the number of employed DC-sources, in single and multiple DC-sources topologies [8] and [9]:

2.2.1 Single DC-source

Researchers applied the concept of multilevel conversion by developing different converter topologies. These topologies aimed to enhance the converters' structural complexity, power losses, and harmonic distortion. A single source topology employs one DC-source as a main voltage reference and uses a set of capacitors to generate the secondary voltage references. Among the most-famous first-generation multilevel inverters are:

1. Neutral Point Clamped inverter (NPC) is a second type of single DC-source converter that employs a neutral point reference between capacitors.

2. The Flying Capacitors inverter (FC) which uses several capacitors, single DC-source, and several switches to generate the required voltage levels. FC simplifies filter requirements, simplifies voltage level generation and control through state redundancies, and provide the possibility to control active and reactive power flow in the system, but the disadvantage is difficult voltage balancing of the capacitors.

3. The Modified Cascaded H-Bridge (MCHB) has single DC-source and additional capacitors in one of its topology variants. This topology has simplified structure, easy maintenance, and simple structure extension process through which the number of voltage levels can be raised.

Moreover, these topologies appeared as the first generation of MLIs with improved reliability and output voltage harmonic response. However, to achieve these advantages, they use high number of components especially diodes in NPC, capacitors in FC, and power switches in MCHB, so it increases size and complexity of control [10],[11], as depicted in Figure 2-1. Research work on Multilevel converters (MLC) and MLI continued to raise benefits and attenuate disadvantages.

a)   b)
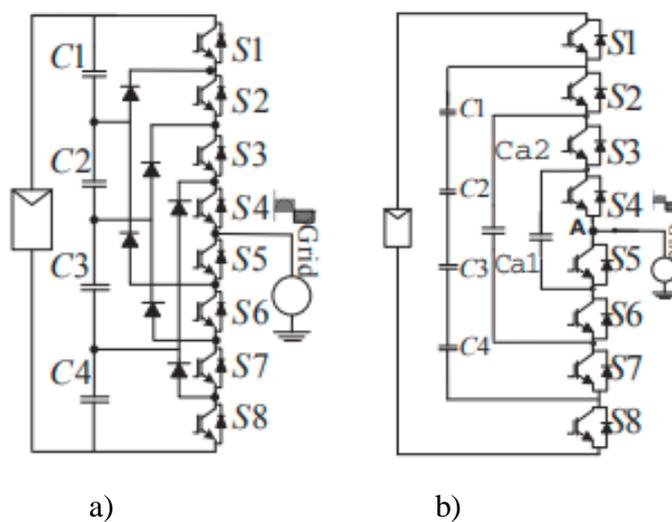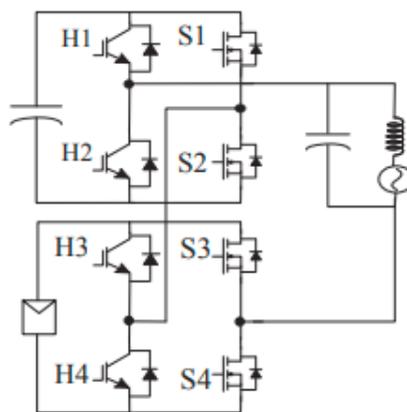
c)

Figure 2-1: Conventional single DC-source MLI topologies: a) NPC b) FC. c) Modified

CHB [9].

Switched-capacitor (SC) is a compact structure that enhances voltage boosting capability, this topology uses capacitors and capacitor charging balancing techniques to achieve required voltage values of capacitors. Several topologies were developed based on SC, among these are the Switched-Capacitor Module (SCM), Figure 2-2(a) [12], Single Stage Switched-Capacitor Module (S^3CM), Figure 2-2(b), and Developed Switched Capacitor Circuit (DSCC), Figure 2-3. The original topology, SCM, has a double-stage modular structure that employs an H-bridge as a second stage to generate the required positive and negative voltage levels. Despite its voltage-boosting advantage, SCM was not scalable to generate higher number of levels. S^3CM used a single-stage topology by eliminating the H-bridge. This topology has both voltage gain and scalability features; however, it has a higher number of components and structural complexity than SCM [13].

DSCC includes two- stage structure with H-bridge as SCM, it achieves nine-level staircase output with only one voltage source, fewer power switches, and capacitors with self-voltage balancing ability. Despite DSCC improved the voltage gain boosting, it lost the scalability and structure extension features of S^3CM [14].
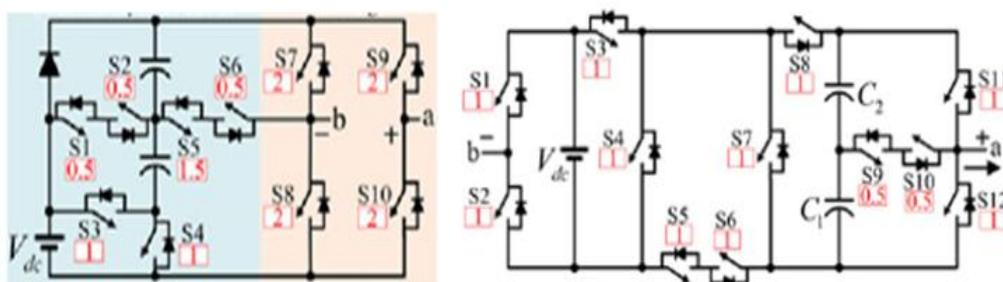
Figure 2-2: Other reduced switches count SC topologies: a) Traditional SCM topology.

b) S3CM: The modified structure of SCM [12],[13]
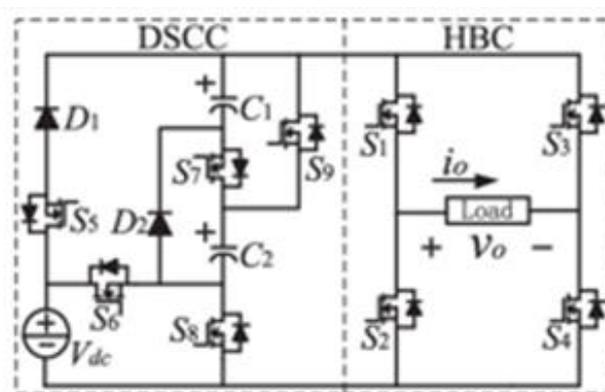
Figure 2-3: SC with H-Bridge structure: DSCC inverter [14]

2.2.2 Multiple DC-sources and Hybrid Topologies

Using several DC-sources is a traditional method to generate multilevel convertors, Multiple DC source topologies are using of cascaded of same

topologies. Conventional CHB is one popular MLI's with multiple isolated DC-sources [15], as shown in Figure 2-4.
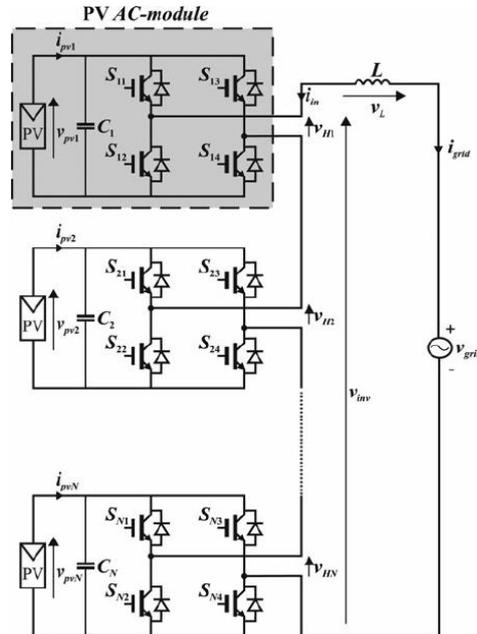
Figure 2-4: Cascaded H-Bridge with separated DC-sources [15]

In [16], Hybrid topologies integrate:

A – Two different topologies or more.

B – Structural changes by adding components or a composition of two or more devices such as diodes or switches to enhance the power losses and THD.

An example of hybrid inverter, the compound structure T-type which consists of two capacitor of DC-link, two unidirectional switches, and a bidirectional switch, this structure is used mostly in hybrid topologies without the two unidirectional switches. Among these topologies are the T-type and cascaded CHB topology proposed in [9], [17], and [18].

Researchers also inspected the possibility of using modular and hybrid design principles to develop other converter topologies. Modular Multilevel Converters (MMC) employ cascaded of similar modules to increase the number of voltage-

levels and implement additional power systems devices such as variable AC voltage-source [19], and [20].

A cascaded multilevel inverter topology that uses a hybrid technique (CMLI) has been illustrated in [21], [22] and [23]. This topology is composed of an addition/subtraction module and a full H-bridge. The first module generates the positive voltage levels, while the second reverses the polarity to generate a complete AC voltage signal. CMLI has three arms, each arm has nine switches and two DC voltage sources, each switch has a single freewheeling diode, and it means big count of components especially the switches for nine-levels. Moreover, the circuit needs nine gate drive circuits, two separate DC voltage sources, a sharing module to reduce the total switches count for all voltage level generation cells, and multiple active switches per state.
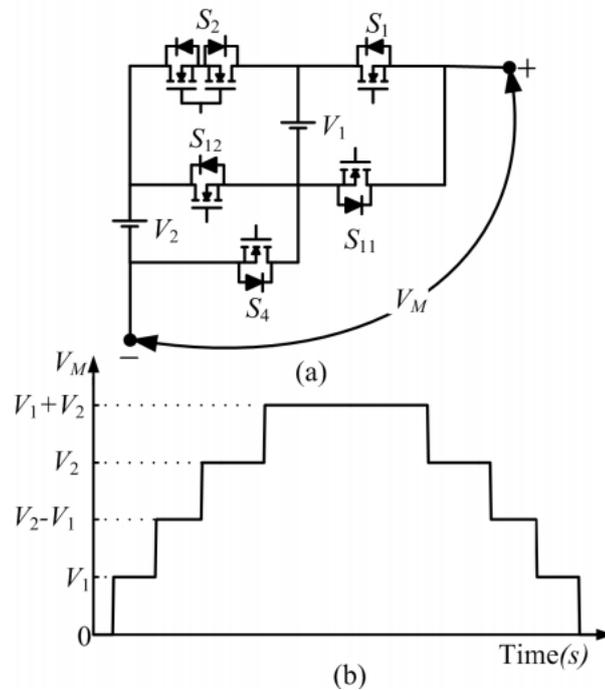
Figure 2-5: CMLI: a) Voltage levels module b) The leveling signal in single CMLI arm

New emerging hybrid structures are now considered the gold-star of multilevel converter topologies. Among these are the basic Packed U-Cell (PUC), Figure 2-6 a), and its variants such as Modified PUC (MPUC), Crossover Switches Cell (CSC), and Packed E-Cell (PEC) as shown in Figure 2-6 b) and c), respectively. PUC combines the FC and CHB topologies or an intersection of a half-bridge and full-bridge modules. The basic U-Cell (an open-circuit half-bridge) is composed of a capacitor and two power switches that controls the charging/discharging process of the capacitor. Despite its advantages, PUC has no voltage-boosting capability, high number of activated switches per voltage level, and a high increase in structure complexity for a small increase in number of voltage levels. It also needs a complex capacitor voltage-balancing technique [24]-[28].

MPUC has a voltage boosting capability. However, it shares with PUC the activation of high number of switches per step voltage [29].

CSC has an enhanced voltage boosting gain with respect to MPUC. However, it requires eight switches (four active switches in ON-state), so the use of a more sophisticated control technique in standalone connection [30], besides its structure was redesigned with Grid-connected application by replacing two unidirectional switches with two bidirectional switches in [31] as illustrated in Figure 2-6 b).
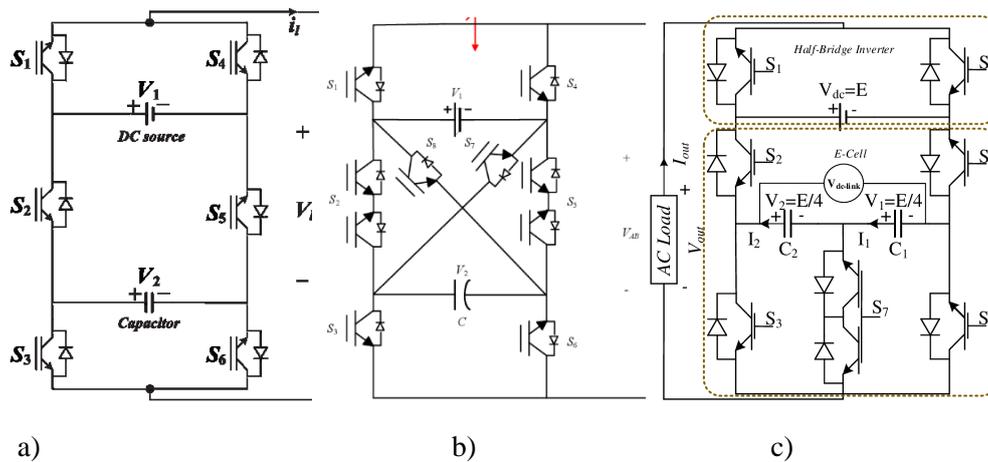
Figure 2-6: PUC family: a) 5 and 7L-PUC. b) CSC. C) PEC9

Packed E-Cell is a modified PUC that uses simplified capacitor voltage balancing technique, reduced component-count and activated switches per level. However, it has no voltage-boosting capability and higher structural complexity, Figure 2-6 c) [32].

Another modified scheme of PUC topology is the seven-level improved PUC (IPUC7), this PUC uses additional switches to achieve voltage boosting capability, it consists of nine switches, single DC-source, and a capacitor as shown in Figure 2-7 [33].
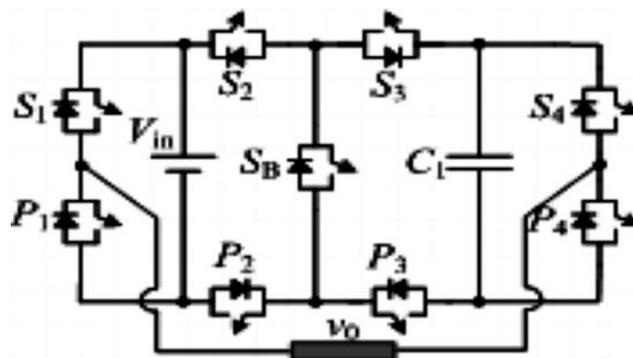
Figure 2-7: IPUC7 schematic [33]

A nine-level cascaded multilevel inverter based on switched-capacitor has been introduced in [34], this topology cascades two SC cell, each of which is composed

of a separated DC-source, a capacitor, a diode, two power switches, and H-bridge. Thus, the structure employs high number of components [35] and [36].

A Cascaded Switched-diode Multilevel Inverter (CSD) for renewable energy integration is presented in [37], CSD inverter has been proposed for medium voltage renewable energy integration as shown in Figure 2-8. CSD topology has many features such as reduced switches count, very simplified control using single switch modules of half bridge that means added single switch in additional modules. However, it has lost level (subtraction levels) as (V_{main1}-V_{main2}) and it needs more components for higher voltage levels.
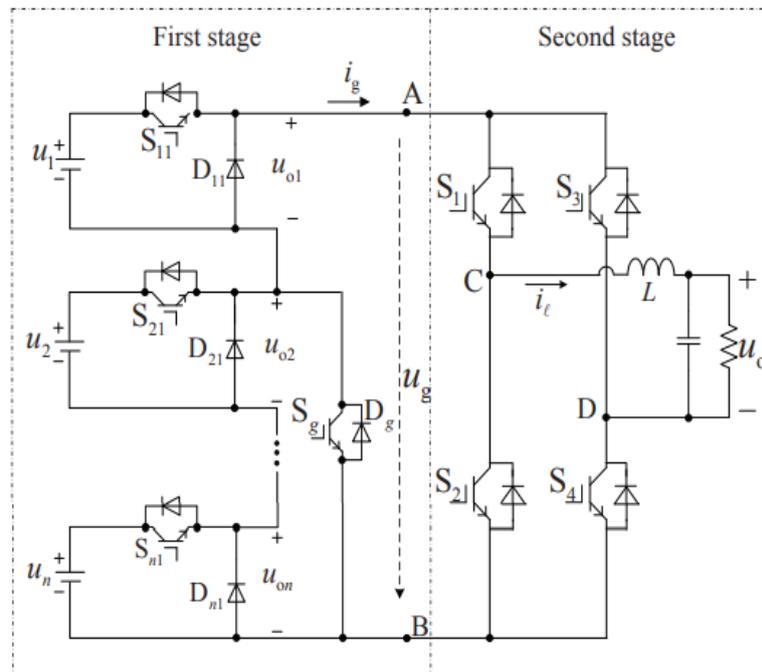
Figure 2-8: The structure of two-stage CSD topology

Total harmonic distortion (THD$_h$):

The ratio of the root mean square of the harmonic content, considering harmonic components to the fundamental component of *h*, THDv when the parameter of contents is voltage, and THDi for the current component, it refers to distortion ratio in the waveform, these parameters are assigned by IEEE std 519 standard, equation (2-1). In power systems, lower THD value means several advantages such as lower losses and so higher efficiency [38].

$$THD_h = \frac{\sqrt{h_2{}^2 + h_3{}^2 + h_4{}^2 + h_5{}^2 + \ldots}}{h_1} X\, 100\% \qquad (2\text{-}1)$$

Where h is the harmonic content of the voltage or current, for voltage h=V, and current h=I.

One of solutions to reduce THD is by increasing the output voltage levels number, more levels that allow the output voltage to become smoother and close to sinusoidal, so the harmonics reduce [39].

In summary, the literature review showed that the existing converter topologies compete in the number of employed components (sources, switches, diodes, and passive elements), single or multiple DC-source, number of voltage levels and activated switches per ON-state, voltage boosting, structural scalability, and complexity of their control techniques.

According to [40], there are many parameters that have to be tackled in multilevel converter design; the most salient issue is the number of employed components. The Reduced Component Count Strategy (RCC) looks to enhance the employment of the following:

- Switches & diodes: the use of a lower number of gate drives may lead reducing the number of switches or diodes. This aims to minimize power losses,

use of smaller packaging, decrease cooling system requirements, and simplify the switching control and voltage balance in added capacitor.

- Sources: the RCC scheme must decide to opt for single or multiple DC-sources with symmetric or asymmetric source configuration. Lower sources count means lower cost; however, it requires the employment of additional capacitors and use of capacitor voltage balancing. Using asymmetric ratio increases the number of output voltage levels and number of redundant. Redundant states can be used to simplify capacitor voltage balancing by the adoption of suitable control techniques. This leads to reduce components number and capacitor voltage-ripple, which means lower THD ratio.

Despite its limitations, RCC has several limitations such as in case of using diodes: The disadvantage of diode is forwarding voltage (V_f), it can be solved by diode with lower V_f. Moreover, the voltage spikes are produced sometimes through unidirectional power flow in high inductive loads because of using diodes in the topology; this is solved by using an LC-filter, such as shown in CSD, Figure 2-8 [37]. Therefore, the design has to be based on the best compromise between these advantages and limitations.

This thesis proposes a modular-scalable hybrid converter topology called Modular Added Cell, MAC, which is structured from three modules, which are called α, β, and γ. The first two modules generate the voltage levels, and the third is for reversing polarity to achieve the negative half-cycle of output voltage. MAC topology has two major structure; the Basic-MAC (α and γ), and the Extended-MAC which has two forms: the first is obtained by repeatedly adding β modules to

the basic structure and the second is composed by using repeatedly connecting α modules with a final γ module that generates full semi-sine wave. Both MAC basic and extended structures are shown to be competitive with existing topologies. In fact, they have improved structural complexity, sources and other components count, and number of active switches per voltage-level.

When compared with several converter structures reported in literature such as PUC, the proposed topologies shown to have enhanced voltage boosting capability, enhanced structural-scalability, reduced number of switches and active switches per voltage level, and the improved ability in achieving higher number of voltage levels with respect to the relative increase in component count. These characteristics can lead to an enhancement in power losses and THD reductions.

Moreover, this study illustrates some Stand-alone and Grid-connected modes of the proposed MAC structures. Two control strategies were employed.

1. For Stand-alone mode, two cases are presented; the first is an open-loop sinusoidal pulse width modulation (SPWM) control for proposed inverter using DC-sources without any auxiliary capacitor, and the other case is closed-loop model predictive control (MPC) for Nine-level MAC with a single DC-source and capacitors.

2. The Grid-connected mode based on a predictive control (MPC) for nine, seven, and eleven levels MAC with a single DC-source and capacitors, also this part shows some step change scenarios on specific parameters to validate the proposed control behavior of eleven-level MAC.

In the chapter 3, the proposed MAC's modules and its generalized MAC topology family schematics are presented, it has three major modules in two forms: α, β, and γ. Beta cell is divided to three types.

CHAPTER 3
THE PROPOSED MODULAR ADDED CELL TOPOLOGY (MAC)

The proposed hybrid converter is characterized of three main modules; α, β, and γ. The first two modules generate the voltage levels, and the third is for reversing polarity to achieve the negative half-cycle of output voltage. MAC topology has two major structure:

- Basic-MAC (α and γ)

- Extended-MAC (xMAC) which has two forms: the first is obtained by repeatedly adding β cells to the basic structure and the second is composed by using repeatedly connecting α modules with a final γ module that generates full semi-sine wave, these added cells include the three types of Beta, and added alpha modules in cascaded and intersected connections.

3.1 MAC's Modules

α, β, and γ modules generate together the multilevel voltage signal near sine wave shape using minimum number of switches and sources for maximum levels. MAC can work in two configurations based on asymmetric voltage references ratio and DC-source count; multiple DC-sources (M-DCS) or a single DC-source configuration with flying capacitors (1-DCS), α and β modules have the role of positive voltage level generation modules, γ is the polarity-reversing module to produce the negative half-cycle of inverter output (V_{inv}), as depicted in Figure 3-1.
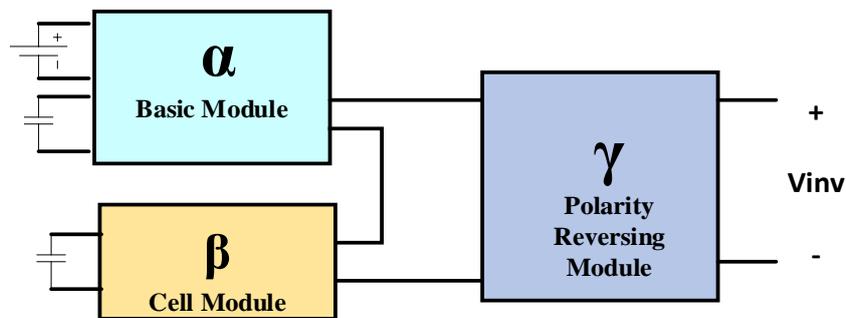
Figure 3-1: General block diagram of the proposed MAC converter with extra β cell module

3.1.1 Alpha-Module (α)

The α-module generates the voltage states and γ -module controls the polarity of the output voltage. The topology operates with two DC-voltage references; the first, V_{main} is a dc-source and the second, V_{sec}, can be a DC-source forming a two DC-source topology or a capacitor in a single DC-source topology, as depicted in Figure 3-2.

This module generates positive levels in asymmetric and multiple sources configurations with ratio $V_{sec} = V_{main}/3$ and $V_{sec} = V_{main}/2$ when it is used in the single alpha module form with i and j nodes connected. In the first and second cases α generates five and four different switching states $(N_{L,\alpha})$, respectively. However, one of these switching states is redundant, produces the same voltage level. Thus, the actual voltage-levels $(V_{o,\alpha})$ produced in each case, as depicted in Figure 3-3, are 4 and 3, respectively.

Figure 3-2: α-module schematic

| a) | b) |
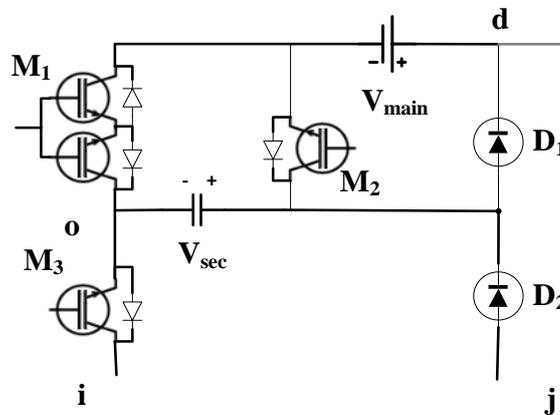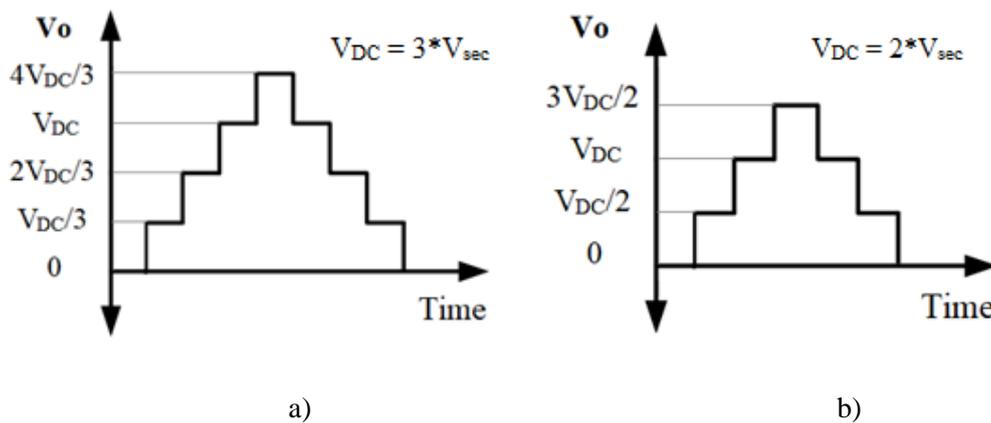
Figure 3-3: Typical waveform of α-module output voltage ($V_{o,\alpha} = V_{uy}$), where $V_{main}=V_{DC}$,

a)MAC9 ($N_{L,\alpha}$= 4) b) MAC7 ($N_{L,\alpha}$= 3)

The switching states and generated voltage levels of the Alpha module are shown in Table 3-1, the first right column includes the state of capacitor which refers to charging, discharging, or bypass in single DC-source configuration. For example, Table 3-1, state 4 refers to the path that produce level equal to $+ V_{sec}$, in this state the switches: M_1 and M_2 are off, and M_3 is On, the diodes D_1 is On and D_2 is Off, the capacitor process is discharging in case of single DC-source configuration. M_1, the bidirectional switch includes two series IGBT, each one has a antiparallel diode, the gate drive of M_1 has role of firing the IGBT as state requirement, M_1 is 1 means: down IGBT is on and upper one is off in positive half-cycle, and vice versa in negative half-cycle.

Table 3-1: Voltage levels generate by α-module activation sequences

	Voltage Level ($V_{o, \alpha}$)	M_1	M_2	M_3	D_1	D_2	C * For single DC-source
1	$V_{main} + V_{sec}$	0	1	1	Off	Off	D
2	V_{main}	0	1	0	Off	On	B
2R	V_{main}	1	0	1	Off	Off	B
3	$V_{main} - V_{sec}$	1	0	0	Off	On	C
4	$+ V_{sec}$	0	0	1	On	Off	D

* B/C/D: Bypass, charging, and discharging of single DC-source MAC's capacitor

3.1.2 Beta-Cell (β)

This cell has three different types; Beta-1 ($β_1$), Beta-2 ($β_2$), and Beta-3 ($β_3$). These modules have a reduced number of components based on simplified half H-bridge structure. $β_1$ is composed of a single unidirectional power switch, a power

diode, and a single dc voltage-reference, Figure 3-4 (a). β_2 is composed of a bidirectional switch, a unidirectional switch, a single power diode, and a single DC voltage-reference, Figure 3-4 (b). β_3 is composed of two unidirectional switches and two power diodes, and a single DC voltage-reference, Figure 3-4 (c).

The proposed cell structure of three Beta types added cells are also shown in Figure 3-4. An Extended-MAC topology with N added cells includes N+2 voltage-references. These voltage-references can be all DC-sources as in the multiple DC-source topology or a single DC-source with a set of capacitors as in the single DC-source topology.

The switching states and generated voltage levels of the three beta cells are shown in Table 3-2, Table 3-3, and Table 3-4, respectively. For example, in Table 3-2, state ($+ V_{sec}$) refers to the path that produces level equal to $+ V_{sec}$, in this state the switch M_N is ON and the diode D_N is OFF, the capacitor process is discharging in case of single DC-source. This process is the same for Table 3-3 and Table 3-4.
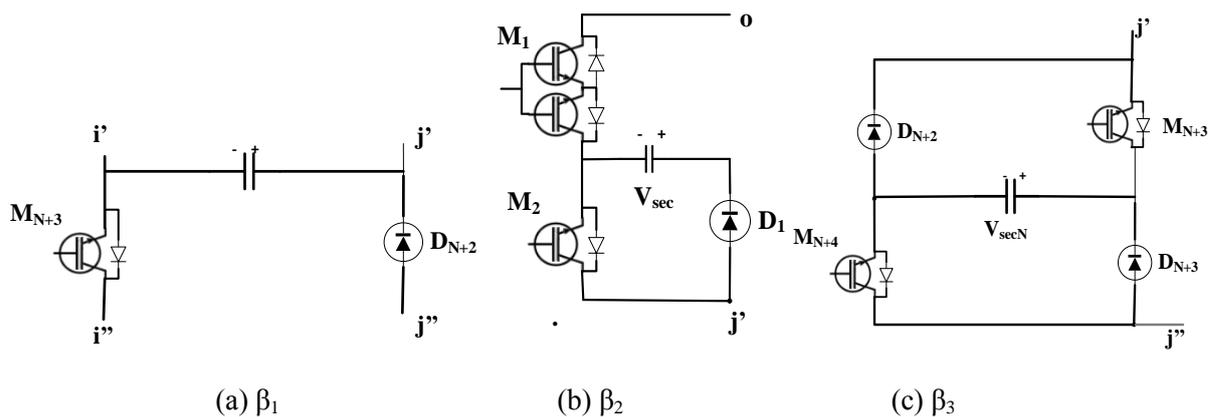
Figure 3-4: Types of β-cells: (a) Beta-1 (b) Beta-2 (c) Beta-3

Table 3-2: Voltage level states generation by $β_1$ activation sequences

Voltage Level (Vo, β)	M_N	D_N	C * 1-DCS configuration only
+ V_{sec}	1	Off	D (path via V_{sec})
0	1	Off	B (path isn't via V_{sec})
0	0	On	B (path isn't via V_{sec})
- V_{sec}	0	On	C (path via V_{sec})

* B/C/D: Bypass, charging, and discharging processes of MAC's capacitor

Table 3-3: Voltage level states generation by β_2 activation sequences

Voltage Level (Vo, β)	M_{N-1}	M_N	D_N	C * 1-DCS configuration only
+ V_{sec}	0	1	Off	D (path via V_{sec})
0	1	1	Off	B (path isn't via V_{sec})
0	0	0	On	B (path isn't via V_{sec})
- V_{sec}	1	0	On	C (path via V_{sec})

* B/C/D: Bypass, charging, and discharging processes of MAC's capacitor

Table 3-4: Voltage levels generated by β_3 activation sequences

Voltage Level (Vo, β)	M_N	M_{N+1}	D_N	D_{N+1}	C * 1-DCS configuration only
+ V_{sec}	1	1	Off	Off	D
0	1	0	Off	On	B
0	0	1	On	Off	B
- V_{sec}	0	0	On	On	C

* B/C/D: Bypass, charging, and discharging processes of MAC's capacitor

3.1.3 Gamma-Module (γ)

Alpha module and Beta cells are voltage level generation cells in positive values, but the desired sine wave has positive and negative half-cycles. An H-bridge (γ-module), Figure 3-5, is used to generate the negative half-cycle. The negative voltage-levels are produced by the complementary operation of H1, H_4 and H_2, H_3, switches as shown in Table 3-5.
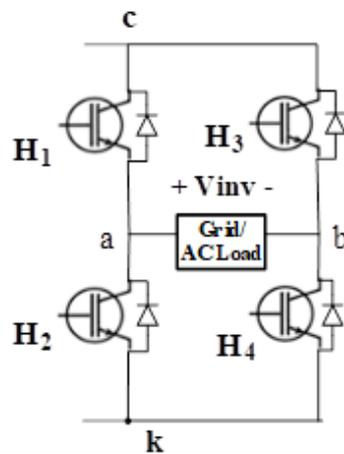
Figure 3-5: γ-module (H-Bridge)

Table 3-5: Gamma-module states

Voltage Level (Vo, γ)	H_1	H_2	H_3	H_4
+ Load	1	0	0	1
0	1	1	0	0
- Load	0	1	1	0

3.2 Basic and Extended MAC TOPOLOGY

The MAC topology has a modular-scalability feature that enables the Basic-MAC and Extended-MAC structures to compete with several existing multilevel modular converters MMC.

Basic-MAC has only Alpha and Gamma modules and can generate nine, seven and five voltage levels based on the symmetric/asymmetric references and references voltage values.

MAC structure can be summarized as a structure from three modules, which are called α, β, and γ. MAC topology has two forms; the Basic-MAC (α and γ), and the Extended-MAC which has two forms: the first is obtained by repeatedly adding β modules to the basic structure and the second is composed by using repeatedly connecting α modules with a final γ module, Figure 3-6.
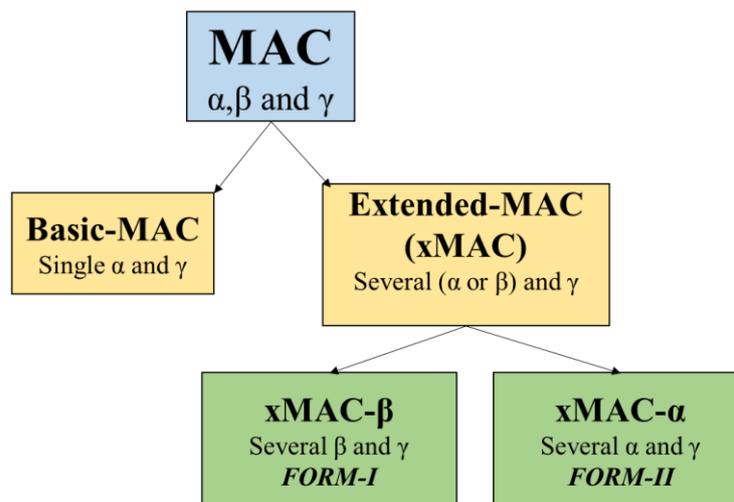
Figure 3-6: General MAC Structure Diagram

3.2.1 Basic Topology of MAC

The hybrid single-phase basic-MAC topology is composed of two modules α and γ, Figure 3-7. The connections between the two modules must be (d-c) and (i-

j-k). The value of V_{main} determines the voltage peak value, whereas, V_{sec} sets the symmetric or asymmetric configuration of operation of the converter. The coordinated operations of α and γ modules lead to the generation of the multilevel staircase approximation of the desired sinusoidal waveform. The following subsections illustrate the structure and principles of operation of the basic-MAC.
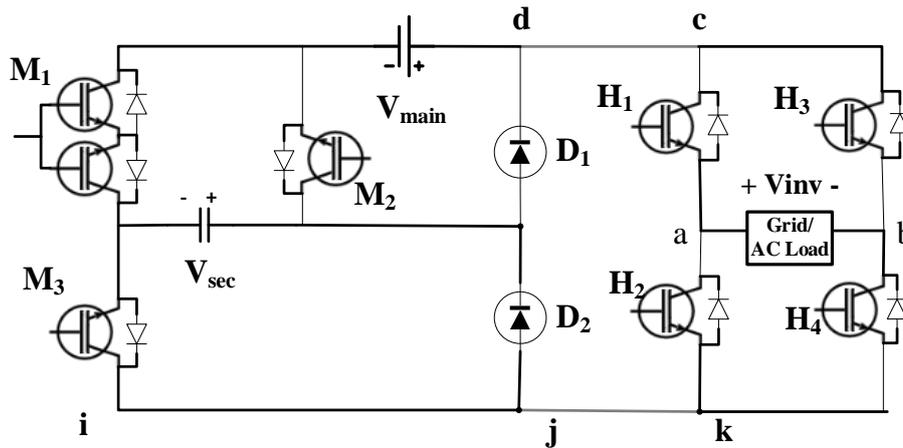
Figure 3-7: The proposed basic topology of MAC, showing the basic α and γ modules

The basic-MAC structure is composed of seven power switches, two power diodes, and two DC voltage-references distributed in two modules, the α and γ modules. The α module is composed of one bidirectional, M_1, two unidirectional (M_2, M_3), power switches with antiparallel diodes, two power diodes (D_1, and D_2), and two DC voltage references, V_{main} and V_{sec}. V_{main} can be a battery in photovoltaic application, the value of V_{main} sets the converter power rating, the voltage peak value and the step-voltage value.

The nature of component that generates V_{sec}, a capacitor or a DC-source, sets the Basic-MAC operation as a single or two DC sources topology, which affects the converter control strategy. The value of V_{sec} is always set as the ratio of V_{main}

that enables the generation of the desired number of voltage-levels. When this ratio is one the converter operates in symmetric configuration otherwise it operates in a asymmetric configuration that depends on the ratio of the two reference voltages. The capacitor values are found in chapter 5 for single DC-source configuration.

The diodes don't need control signal, this gives simpler and lower switches count for same number of levels in this topology. Alpha-module requires a bidirectional switch (M_2) with conducting current in both directions and voltage blocking capabilities [43]; this bidirectional switch is necessary to prevent the short circuit path via this M_2 if a unidirectional switch is used when states of V_{main} or -V_{main} is active, and for two direction current flow, there are three types of bidirectional switch [44]:

1. IGBT with quad diodes (4D-IGBT) as shown in Figure 3-8 (left).

2. A reverse blocking IGBT (RB-IGBT) which has two IGBT with common connection as the collector of first IGBT is connected to emitter of the second one and these are also applied on other IGBT, each IGBT has intrinsic diode as depicted in Figure 3-8 (middle).

3. CE-IGBT Scheme based on two series IGBT with common emitter connection, also each IGBT has a antiparallel diode, as Figure 3-8 (right) shows.
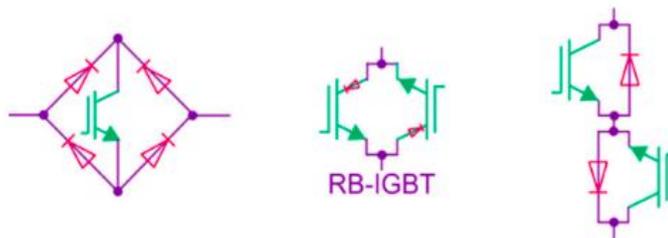
Figure 3-8: Bidirectional switches based on IGBT [44]

The third type is used in the proposed MAC inverter validations due to:

- 4D-IGBT has four diodes, so it requires high components count.

- The RB-IGBT which has lower switching loss than series connected IGBTs, this type can be used instead of CE-IGBT for MAC, especially in case of losses reduction study, but this thesis presents the proposed structures and it based on RCC strategy, so type 2 and 3 can be used in MAC structure with same principle of operation.

The γ-module is composed of four unidirectional power switches (H_1, H_2, H_3 and H_4) with anti-parallel diodes. The switches (H_1, H_4) and (H_2, H_3) form two groups that operate in a complementary configuration. It is an H-Bridge that connects the inverter output-nodes (a, b) to the power grid or AC load, Figure 3-7. The γ-module controls the polarity of the staircase output voltage V_{inv}, for zero state is produced when $H_1=1, H_2=1, H_3=0, H_4=0$.

The name refers from its topology concept of different connected modules. Topology of the proposed single phase nine-Level MAC without extra cell modules (β), basic MAC can generate 5-Level, 7-Level, and 9-Level voltage signals in M-DCS and 1-DCS configurations. The following subsections will introduce the Extended-MAC (xMAC) structure and its operation principles and voltage-level generation process. MAC can be employed as an MMC with a modular scalability feature, it can operate as a controlled voltage source [19].

3.2.2 Extended-Topology of MAC (xMAC)

This section proposes two forms of generalized modular-scalability of Extended-MAC (xMAC); these forms follow the approach introduced in [19].:

- The first, Form-I uses a β-module as a modular added cell to extend the Basic-MAC structure, Figure 3-9 (a). The resulting xMAC topology has a modular cascade topology composed of a single α-module, a sequence of same-type β-cell, and a final polarity control γ-module.

- The second, Form-II uses a cascaded or intersected modular structure of α-modules with a final polarity control γ-module. Form-II inherits all the advantages of the Basic-MAC topology, Figure 3-9 (b).

- The modular extension of the Basic-MAC with Form-I can be achieved using all the proposed types of β-module.
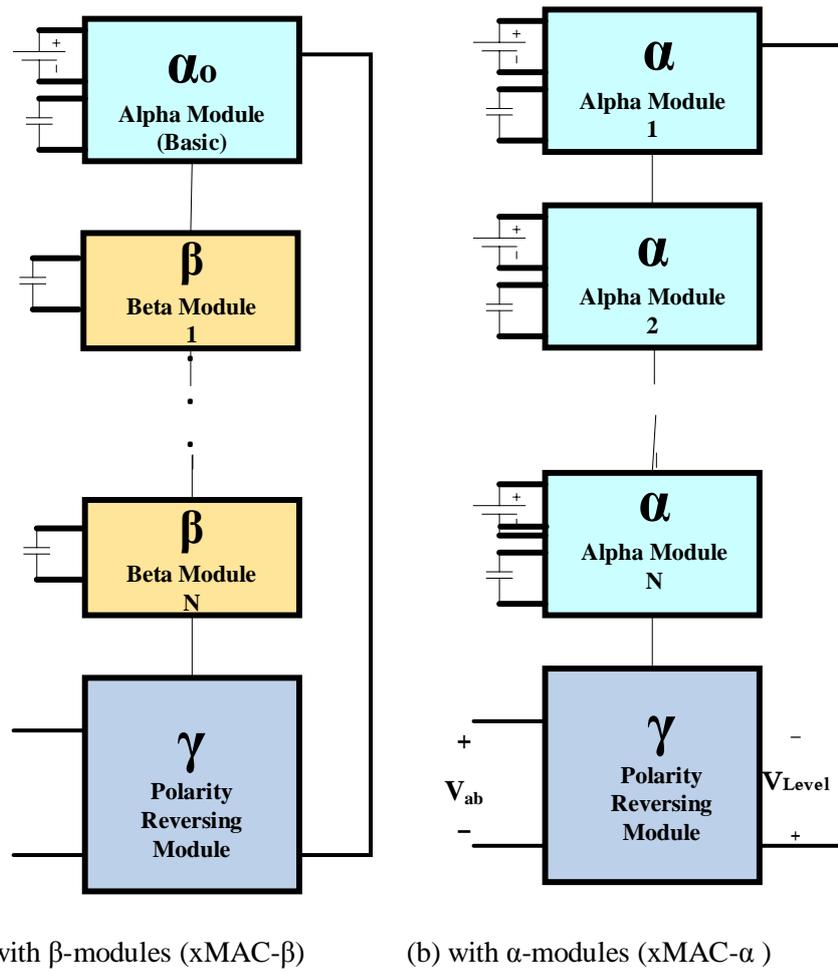
(a) with β-modules (xMAC-β) (b) with α-modules (xMAC-α)

Figure 3-9: Block diagram of generalized MAC topologies. a) Form-I: xMAC with added

β-modules. b) Form-II: xMAC based on cascaded or intersected α modules

3.2.2.1 xMAC with the three types of Beta-cells (xMAC-β)

In previous chapter, the extendibility of MAC is presented using three Beta-cells, also this part describes several Extended-MAC topologies in the mentioned two sources ratio configurations.

A. MAC with β₁-cell (xMAC-β₁)

This MAC-β_1 is consisting of three modules (alpha, intersected beta-1, and gamma) in two configurations: M-DCS and 1-DCS, the connections between

MAC modules are shown in Figure 3-10, the connections between the three modules (α-β-γ) are: (d-c), (i-i'), (j-j'), and (i''-j''-k).
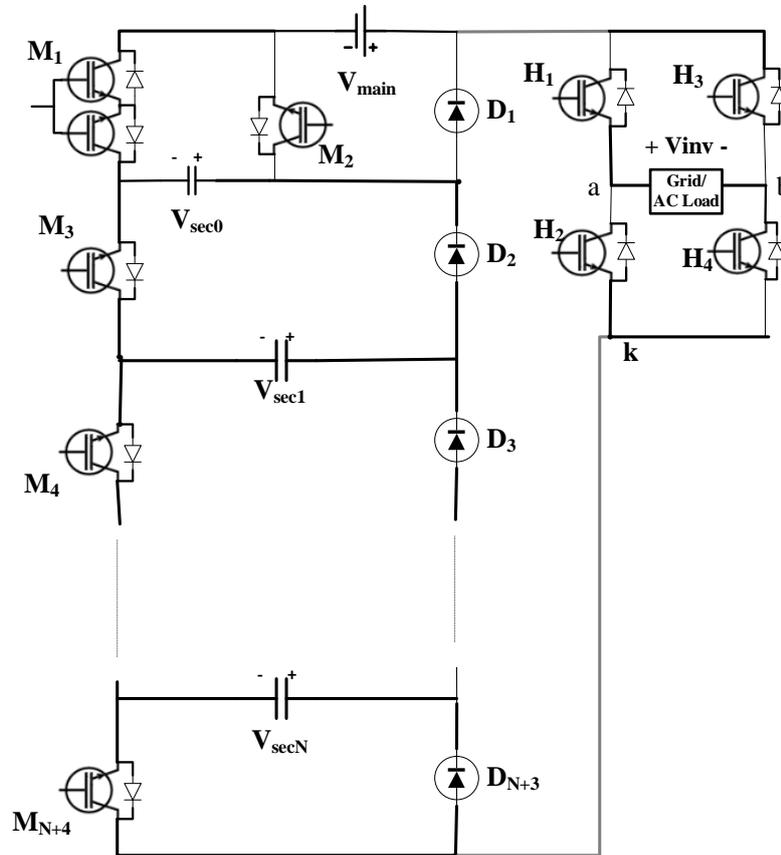
Figure 3-10: Generalized xMAC-β₁ schematic

B. MAC with β₂-cell (xMAC-β₂)

This MAC-β_2 is consisting of three modules (alpha, intersected beta-2, and gamma) in M-DCS configuration which is selected configuration due to verifying the operation.

In this configuration; all secondary voltage-references (V_{sec0}, and V_{sec1}) are DC-sources, the connections between MAC modules are shown in Figure 3-11.
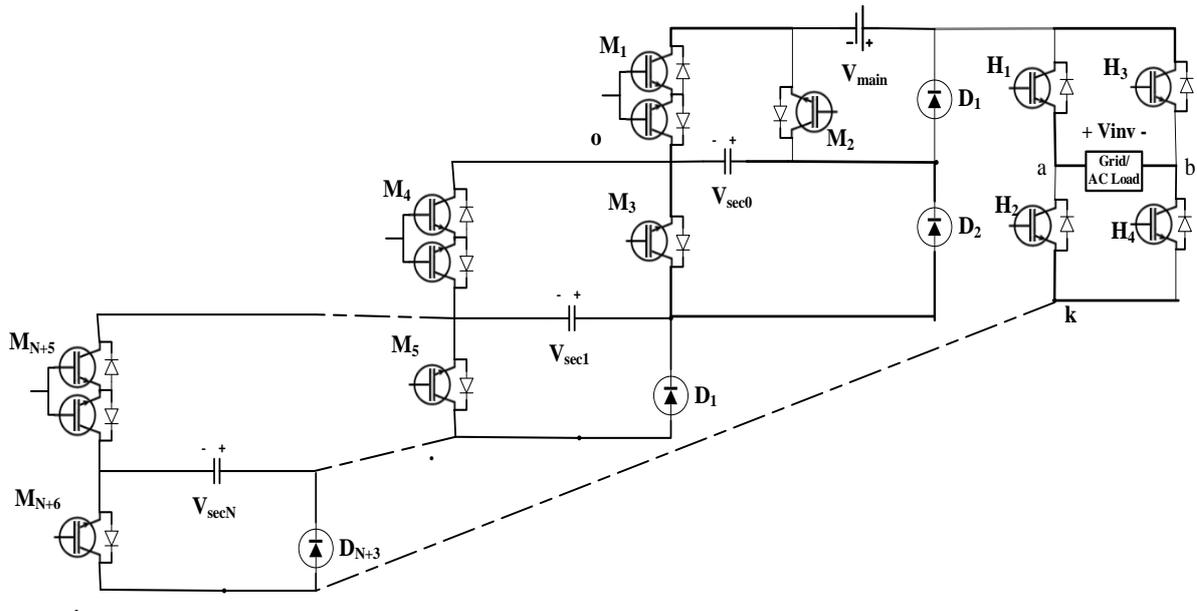
Figure 3-11: Generalized xMAC-β₂ inverter schematic

C. MAC with β₃-cell (xMAC-β₃)

This MAC-β_3 is consisting of three modules (alpha, cascaded beta-3, and gamma) in M-DCS configuration which is selected due to verifying the operation. In this configuration; all secondary voltage-references (V_{sec0}, and V_{sec1}) are DC-sources, the connections between MAC modules are shown in Figure 3-12.

Figure 3-12: Generalized xMAC-β_3 inverter schematic

3.2.2.2 MAC with several Alpha-module (xMAC-α)

This MAC- α is consisting of two modules (several alpha's, and gamma), there are two different connection of added Alpha: cascaded and intersected schemes.

A. MAC with cascaded Alpha-modules (xMAC-$α_c$)

The added Alpha's are connected in cascading as shown in Figure 3-13. In this thesis, M-DCS configuration is selected due to verifying the operation. In this configuration; all secondary voltage-references (V_{sec0}, and V_{sec1}) are DC-sources.

Figure 3-13: General xMAC-α_c schematic

B. MAC with intersected Alpha-modules (xMAC-α_i)

The added Alpha's are connected in intersection as shown in Fig 3-14. In this thesis, the difference between this scheme and last cascaded one is presented. In this configuration; all secondary voltage-references (V_{sec0}, and V_{sec1}) are DC-sources.
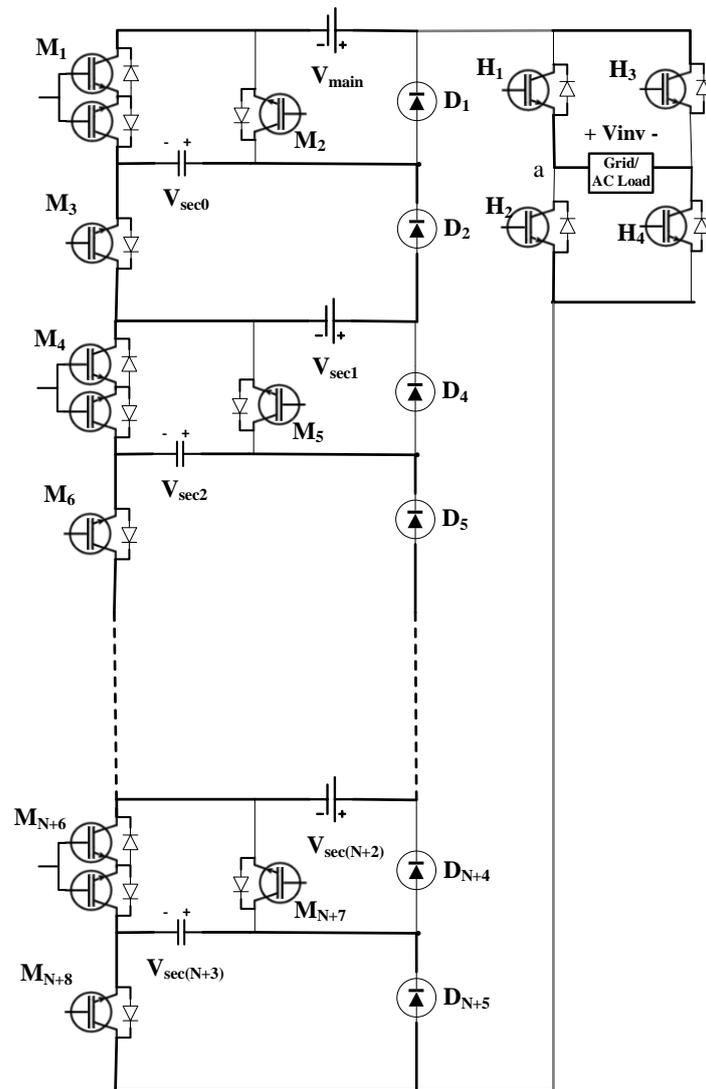
Figure 3-14: General xMAC-α_c schematic

As mentioned before, Second MAC's form includes two schemes of Added Alpha-modules; cascading and intersection. These schemes have several differences which summarizes in 1-DCS configuration, Table 3-6.

Table 3-6: Differences between two xMAC-α schemes in 1-DCS configuration

MAC-α	Ns	Nc	BA*
MAC-α_c	N	N	Yes, and incremental
MAC-α_i	1	N-1	Yes, and constant for N Added α

*Boosting Ability (BA) means Output voltage of MLI is bigger than the biggest input DC sources

By noting, MAC-α_i has the same states of xMAC-$2\beta_1$, but with more redundant state in each added Alpha (for example, (V_{sec1} +V_{sec2}) in two intersected Alpha's, see Figure 3-13, it allows ease voltage balancing of capacitors)

3.3 MAC Codename

The most important feature of the proposed MAC is scalability; this feature gives multiple options in related converter design based on compatible different modular added cells concept. Simplicity is another feature of MAC; the detailed codename of MAC is clear and it illustrates in Figure 3-15.

$$\text{MAC}\boxed{\text{N}_\text{L}} - \boxed{\text{N}}\boxed{\text{T}_\text{C}} (\boxed{\text{X}}\text{-DCS})$$

Figure 3-15: The proposed detailed codename of MAC

Where N_L: Number of desired voltage levels,

N: Number of used modular added cells,

T: Type of added cell (α-modules or β -cells),

C: Number of type (for Added Beta Cell), or connection type (for Added

Alpha module (c or i)),

X: Single or multiple DC-source (1 or M).

For example, **MAC81-2β₃ (M-DCS)** refers to 81-level MAC topology based on two added Beta cells of type 3, and the asymmetric voltage-references configuration is Multiple DC-source. Other example is **MAC9 (M-DCS)** refers to 9-level MAC and with M-DCS configurations. Also, **MAC49-2α_c (1-DCS)** refers to 49-level MAC with cascaded double Alpha and 1-DCS configuration. By noting that MAC with 1-DCS configuration can operate using multiple DC-sources, but MAC with M-DCS can't operate with a single DC-source connection in desired levels number and shape expect MAC9 (M-DCS), so **Single DC-source MAC9 (M-DCS)** in case of MAC9 with a single source.

In next chapter, MAC features are described in details, the feature of voltage gain is analyzed mathematically, the derivate forms are basic and extended structures based on three MAC modules. Also, it gives the equations that find the number of levels for each form, voltage-references values for all levels, and other parameters. A comparison between MAC verses other competitors for several parameters such as switches and sources count.

CHAPTER 4
MAC: PRINCIPLES OF OPERATION AND FEATURES

This chapter shows how to calculate the following parameters of each MAC forms for added N-cells mathematically, and in two DC-source configurations (1-DCS and M-DCS):

-   Voltage levels number (N_L).

-   Values of V_{DC} and V_{sec} reference-voltages in each case.

-   Total components count for each MAC's structure such as number of total needed diodes (N_D), switches (N_{SW}), and capacitor (N_C) in each structure.

Also, the last part illustrates the difference between MAC with the three types of beta briefly, it gives summaries total components count of xMAC-β form for first three added beta cells of each type, and the second form (xMAC-α) for first three cascaded added alpha modules. Also, it describes the major features of MAC, and it illustrates the needed equations of these features. After that, the differences are determined between the added-cells (Beta's and Alpha's) based on some parameters such as levels count and voltage gain.

At the end, a comparison is based on single DC-source and same number of levels; between the proposed MAC9 (M-DCS) verses other nine-level competitors based on the following parameters:

- Components count such as switches and source number for nine level topologies

- Active switch count per state.

Other comparisons, switch count of xMAC (1-DCS) verses PUC for N-cells and with same capacitor number (N_C), basic single DC-source MAC7 (1-DCS) verses IPUC7, and Extended MAC11-β_1 (1-DCS) verses PUC9.

4.1 Basic-MAC Modules Operation

The Basic-MAC output signal is generated by the coordinated-switching of the power switches of α and γ modules. The activation sequences of the power transistors of the Basic-MAC structure, Figure 3-7, can generate the twelve different ON/OFF states shown in Table 3-1. However, some of these states are redundant and generate similar voltage-difference at the output. The number of different voltage levels is related to the value of the secondary voltage-reference V_{sec}.

For this thesis, the cases of asymmetric operation with $V_{sec} = \frac{Vmain}{3}$ in M-DCS configuration and with $V_{sec} = \frac{Vmain}{2}$ for 1-DCS configuration, three of the five states are redundant, Table 3-1. Thus, only nine different voltage levels are generated resulting in a nine-level converter MAC9 for the first M-DCS configuration, a seven-level are generated for a 1-DCS configuration (states 2 to 8R only).

In case of Grid-connected case, voltage boosting capability is essential feature when inverters are designed for RES because of low generated voltage of these energy generation systems, this output voltage isn't high enough boosting to integrate with grid-connected systems [42].

4.2 xMAC Operation and Voltage- Levels Generation

The operation and voltage-levels generation of the MAC topology is based on the coordinated switching of the basic α-module, β-modules, and the polarity control γ-module. It worth emphasizing that the total number of voltage levels generated by the extended-MAC depends on the settings of the basic-MAC, type of the added cell, and total number of added modular cells. In addition, in each case the voltage-reference of the added cell has to be determined from its position in the sequence, the voltage-references of the basic-MAC cell and the number of voltage levels. In the following, the various concepts and features will be illustrated using a basic nine-level MAC structure (MAC9) and the two forms of Extended-MAC topology; three different modules and cascaded alpha forms.

Also, the voltage levels depend on the asymmetric voltage ratios, M-DCS and 1-DCS configurations. M-DCS gives high number of levels, but it requires multiple DC-sources, 1-DCS gives a smaller number of levels verses the M-DCS, and it needs a single DC-source which is a great feature of the proposed MAC.

Other benefit of 1-DCS configuration is redundant states that allow simplifying the capacitor voltage balancing process of charging and discharging, for example, the state $\frac{V_{DC}}{2}$ has two redundant states of seven level Basic-MAC; One has a charging of the capacitor, and the other is a discharging, so the swapping between the two states is very easy and keeping in the desired level:

A. M-DCS Ratio Sequence

This configuration based on two popular mathematical sequences:

- Mersenne-Prime sequence (M-P): 1, 3, 7, 15, 31, …, $2^n - 1$ for Basic-MAC, xMAC-β_1, and xMAC-β_2, such as for single Beta-1; where N=1, n=N+2=3, V_{sec0}, V_{sec1} has $\frac{a_2}{a_3} = \frac{3}{7}$, and $\frac{a_1}{a_3} = \frac{1}{7}$ of V_{main}, respectively.

- A sequence 1, 3, 9, 27, …, 3^{n-1} for xMAC-β_3, where for single Beta-3; where N=1, n=N+2=3, V_{sec0}, V_{sec1} has $\frac{a_2}{a_3} = \frac{3}{9}, \frac{a_1}{a_3} = \frac{1}{9}$ of V_{main}, respectively.

B. 1-DCS Ratio Sequence

It uses sequence 1, 2, 4, 8, 16, …, 2^{n-1} for all forms, where for single Beta-1; where N=1, n=N+2=3, V_{sec0}, V_{sec1} has $\frac{1}{2}, \frac{1}{4}$ of V_{main}, respectively. In next sections, the previous two configurations are illustrated in detailed. The proposed configurations based on sequence elements for N added Betas, as illustrate in Table 4-1 where i start from N+1 to 1 and n=N+2.

Table 4-1: Asymmetric Ratio Configurations for N Added β-cells.

Ratio Config.	Seq. Type	Sequence	Beta Type	Alpha*, **		.	$(N-1)^{th}$ Beta	N^{th} Beta
				V_{main}	V_{sec0} i=N+1	.	$V_{sec(N-1)}$ i=2	V_{secN} i=1
M -DCS	M-P	1, 3, 7, 15, 31, …, $2^n - 1$	β_1, β_2	1	$\frac{2^i - 1}{2^n - 1}$	.	$\frac{3}{2^n - 1}$	$\frac{1}{2^n - 1}$
	Ternary	1, 3, 9, 27, …, 3^{n-1}	β_3	1	$\frac{3^{i-1}}{3^{n-1}}$	.	$\frac{3}{3^{n-1}}$	$\frac{1}{3^{n-1}}$
1 -DCS	Binary	1, 2, 4, 8, 16, …, 2^{n-1}	β_1	1	$\frac{2^{i-1}}{2^{n-1}}$	.	$\frac{2}{2^{n-1}}$	$\frac{1}{2^{n-1}}$

4.2.1 Form I: Added Beta Cells (xMAC-β)

Figure 3-9(a), The total number of levels generated by the addition of N β-cells ($β_1$,

$β_2$, and $β_3$) are presented in Table 4-2. It worth emphasizing that these relations

show a very high rate-increase in the number of voltage levels with a minimal

change in structural complexity and components count.

Table 4-2: Number of levels and component-count in xMAC with N added β-cells. *

Adding to Basic-MAC		Beta-1	Beta-2	Beta-3
V. levels	M-DCS (N_L)**	$2*(10(2)^{N-1}+2((2)^{N-1}-1))+1$ ***	$2*((2)^{N+3}-N-4)+1$ ***	3^{N+2} *
	M-DCS formula	1: 3: 7: 15: 2^n-1		1: 3: 9: 3^{n-1}
	1-DCS (N_L)****	$2*(6(2)^{N-1}-1)+1$***		
	1-DCS (N_L)**** Sources	$2*(6(2)^{N-1})+1$***	$2*(7(2)^{N-1}+N-1)+1$***	
	1-DCS formula	1: 2: 4: 8: 2^{n-1}		
n (# of sequence element)		n=N+2		
N_{SW}*		N + 7	2*N + 7	
N_S * M-DCS config.		N+2		
N_C* 1-DCS config.		N+1		
N_D *		N + 2	N+2	2*N+2

*N = 0 when alpha-module is used only without any β-cell (likes Basic-MAC)

** Voltage-levels are the maximum for each configuration based on MAC sources ratio value and states, without redundant level counts

*** valid for N ≥1

**** N starts from N=1

Also, the equations are derived directly based on last mentioned sequences, but the

number of levels is reduced for 1-DCS configuration, because the higher levels has

not all redundant stats that need to voltage balancing for capacitors. For example, MAC11-β1 is based on 1-DCS ratio, the sequence gives 13 level, but the two levels have not enough redundant states to control capacitors, so number of levels has a suitable derivative equation based on redundant states count.

It is also important to note that the extension added cell modules requires the employment of different voltage addition of the extension modules. In the case of symmetric single source topology, the value of the DC voltage-reference of a given added cell has to be one-half of that of the preceding cell.

A. M-DCS Configuration:

Whereas, in M-DCS configuration, the value of the main DC voltage-reference for N added beta to MAC9 basic topology (N=0) is given by Table 4-2 and n=N+2. In case of using Beta-cells, the equations (4-1) for β_1 and β_2 modules based on the popular sequence 1, 3, 7, 15, …, and equations (4-2) for β_2-module, and equations (4-3) for β_3-module:

$$V_{\text{main, }\beta1} = \frac{((2)^{N+2}-1)*V_{o,peak}}{10(2)^{N-1}+2((2)^{N-1}-1)} \qquad (4\text{-}1)$$

For Extended-MAC with β_2-module:

$$V_{\text{main, }\beta2} = \frac{((2)^{N+2}-1)*V_{o,peak}}{(2)^{N+3}-N-4} \qquad (4\text{-}2)$$

For Extended-MAC with β_3-module:

$$V_{\text{main, }\beta3} = \frac{((3)^{N+1})*V_{o,peak}}{(3^{N+2}-1)/2} \qquad (4\text{-}3)$$

For example, in M-DCS configuration; adding one, two, or three β_1 cells to the basic-MAC module raises the number of switching states (N_L) to 23, 45, and 93, respectively. For adding the same number of β_2 cells, N_L raises to 23, 53, and 114.

While adding the same number of β_3 cells raises N_L to 27, 81, and 243, respectively.

B. 1-DCS Configuration:

However, the increase in number of switching states is not the actual number of generated states because several states are redundant and generate existing voltage levels, but the last counts of voltage levels aren't including redundant sates, so these counts refer to magnifications of the proposed hybrid MAC.

Nevertheless, this redundancy is not useless; in fact, this redundancy is used in the voltage-balancing control techniques to set the redundant similar voltage values with different capacitor-charging states for both Basic-MAC and for Extended-MAC in 1-DCS configuration, which has flying capacitors. Therefore, having higher number of redundant states allows reducing the capacitors' voltage ripple and lower THD. This number of the redundant states depends on the used MAC structure is affected by the symmetry of the voltage references.

In fact, operating the nine-level basic-structure with asymmetric 1-DCS configuration will lead to a seven-level basic-MAC (MAC7). In this case, the value of the DC voltage-reference of the cell at position (N) of the extended MAC7 is given by equations (4-4) for three β-modules:

$$V_{main} = \frac{(2)^{N+1} * V_{o,peak}}{6(2)^{N-1} - 1} \tag{4-4}$$

In this configuration, the redundant states count is increasing with type of Beta-module, such as β_1-extension has lowest number of these states. For example, in 1-DCS configuration with single DC-source; adding new Beta-cell likes β_1 to

achieve the redundant states which have charging and discharging of capacitors that are needed to keep voltage level balancing for these voltage- references. After adding one, two, or three of any Beta cells, the basic-MAC module switching states N_L raised to 11, 23, and 47, respectively.

For this configuration sources ratio in case of using DC-sources as voltage-references of the cell at position (N) with MAC7 basic topology is given by equations (4-5) and (4-6) for β_1, equations (4-7) and (4-8):

$$V_{main} = \frac{(2)^{N+1} * V_{o,peak}}{6(2)^{N-1}} \tag{4-5}$$

$$V_{sec\ (N)} = (\tfrac{1}{2})^N \frac{V_{main}}{2} \tag{4-6}$$

For β_2 and β_3:

$$V_{main} = \frac{(2)^{N+1} * V_{o,peak}}{7(2)^{N-1} + N - 1} \tag{4-7}$$

$$V_{sec\ (N)} = (\tfrac{1}{2})^N \frac{V_{main}}{2} \tag{4-8}$$

For example, after adding one, two, or three of Beta-1 cells, the basic-MAC module raises N_L to 13, 25, and 49, respectively. While adding the same number of Beta-3 cells raises N_L to 15, 31, and 63, respectively.

To keep the illustration clear, simple, and with reduced count of components based on RCC strategy; an Extended-MAC modular structure with a single Beta-1 cell is considered. The switching sequences and their respective generated voltage levels are presented in Table 3-5. Moreover, the power- switches and diode activation states.

Therefore, the inverter output voltage is given by $V_{o,\ peak} = V_u - V_y$. The output voltage-levels generated by the other sequences can be easily deduced following the conduction paths through the activated, ON-state, switches and diodes (dark black-color). V_{inv} is determined by the combination of the path voltage-references taking into account their respective polarities.

The hybrid MAC topology provided similar features and thus can be also employed as a variable controlled source. In fact, changing the length of activated cells in the sequence of β-cells generates a plausible approximation of ac signals with different peak values.

4.2.2 Form II: Cascaded Alpha modules (xMAC-$α_c$)

Form-II in Figure 3-9(b) which is an arm of MMC uses $N_α$ cascaded α modules with single γ module (αγ structure) to achieve higher output voltage levels, the total output voltage (V_o) is:

$$V_{ab} = V_{dj1} + V_{dj2} + \ldots + V_{dj(N\alpha)} \tag{4-9}$$

And the number of total voltages levels is found based on Table 4-3. For example, if two Alpha modules are used in M-DCS configuration and $N_{L,\ α} = 4$, the total number of levels is:

$N_L = 2*((4+1)^2-1) +1 = 49$ voltage level.

And if two Alpha modules are used in M-DCS configuration and $N_{L,\ α} = 3$, the total number of levels is:

$N_L = 2*((3+1)^2-1) +1 = 31$ voltage level

*Table 4-3: Component-count and N_L in generalized Extended-MAC with N added α-modules. ** *

Adding to <u>Basic-MAC scheme</u>		Alpha
Voltage levels	**M-DCS (N_L)***	$N_L = 2* ((N_{L,\,\alpha}+1)^{N\alpha} -1) +1$**
	1-DCS (N_L)**	
Total No. of Switches (N_{SW})		$3N_\alpha + 4$
Total No. of Sources (N_S) [M-DCS configuration]		$2N_\alpha$
Total No. of Capacitors (N_C) [1-DCS configuration in each Alpha]		N_α
Total No. of Diodes (N_D)		$2N_\alpha$

* $N_\alpha = 1$ when main alpha-module is used only without any extra alpha-module

** Where $N_{L,\,\alpha}$ is the number of voltage levels for each Alpha (3 or 4)

*** $N_{L,\,\alpha} = 4$ levels peak for each Alpha

**** Each Alpha-module has a single DC-source, and $N_{L,\,\alpha} = 3$ levels peak

A.   M-DCS Configuration:

The value of the DC voltage-reference of the cell at position (N_α) with MAC basic-topology (which has $N_\alpha =1$) is given by equations (4-10) to (3-15) for N_α added Alpha-module based on cascaded alpha's form and $N_{L,\alpha} = 4$.

Main voltage source value for first alpha (α_o) and start with $N_\alpha = 2$ is for cascaded form by:

$$V_{\text{sec, }\alpha(N\alpha)} = \frac{V_{o,peak}}{(N_L-1)/2} \qquad \text{(4-10)}$$

$$V_{\text{main, }\alpha\,(N\alpha)} = (N_{L,\alpha} - 1)* V_{\text{sec, }\alpha\,(N\alpha)} \qquad \text{(4-11)}$$

$$V_{\text{sec, }\alpha(N\alpha-1)} = (N_{L,\alpha} + 1)* V_{\text{sec, }\alpha\,(N\alpha)} \qquad \text{(4-12)}$$

$$V_{main, \, \alpha \, (N\alpha-1)} = (N_{L,\alpha} - 1)* V_{sec, \, \alpha \, (N\alpha-1)}$$ (4-13)

$$V_{sec, \, \alpha 1} = (N_{L,\alpha} + 1)* V_{sec, \, \alpha \, (N\alpha-1)}$$ (4-14)

$$V_{main, \, \alpha 1} = (N_{L,\alpha} - 1)* V_{sec, \, \alpha \, (N\alpha-1)}$$ (4-15)

Where:

$V_{main, \, \alpha 1}$ the main DC-source value for first Alpha-module.

$V_{sec, \, \alpha 1}$ the sec. DC-source value for first Alpha-module.

$V_{main, \, \alpha(N\alpha)}$ the main DC-source value for N_α Alpha-module.

$V_{sec, \, \alpha \, (N\alpha)}$ the sec. DC-source value for N_α Alpha-module.

B. 1-DCS Configuration:

The value of the DC voltage-reference of the cell at position (N) with MAC7 basic topology (which has $N_\alpha =1$) is given by previous same equations (4-10) to (4-14) for N_α added Alpha-module based on cascaded alpha's form, but they are with $N_{L,\alpha} = 4$.

4.2.3 xMAC Levels & Components Count Summary

Table 4-4, Table 4-5 and Table 4-6 summarize the generated voltage levels and total components count for three types of added beta cells and based on two asymmetric configurations and the component count.

For example, when xMAC-β is composited from three Beta-1 cells the N_L is 11 levels in 1-DCS configuration, and the total component count are: N_{SW} is 8 switches, N_D is 3 diodes, $N_S =1$ main source, and $N_{sec}=2$ secondary sources.

Table 4-4: Summary for xMAC-β with first three different added Beta 1 cells

Added Cell No. (N)	xMAC-β₁						
	N_{SW}	N_D	N_S	N_{sec}	N_L M-DCS	N_L 1-DCS	N_L 1-DCS | Sources
1	**8**	**3**	**1**	**2**	21	11	13
2	**9**	**4**	**1**	**3**	45	23	25
3	**10**	**5**	**1**	**4**	73	47	49

Table 4-5: Summary for xMAC-β with first three added Beta 2 cells

Added Cell No. (N)	xMAC-β₂						
	N_{SW}	N_D	N_S	N_{sec}	N_L M-DCS	N_L 1-DCS	N_L 1-DCS | Sources
1	**9**	**3**	**1**	**2**	23	11	15
2	**11**	**4**	**1**	**3**	53	23	31
3	**13**	**5**	**1**	**4**	114	47	63

Table 4-6: Summary for xMAC-β with first three different added Beta-3 cell

Added Cell No. (N)	xMAC-β₃						
	N_{SW}	N_D	N_S	N_{sec}	M-DCS	1-DCS	1-DCS | Sources
1	9	4	1	2	27	11	15
2	11	6	1	3	81	23	31
3	13	8	1	4	269	47	63

Cascaded alpha modules give high levels count, but it requires for each added alpha three switches, two diodes, and two voltage-references; one of them is a DC-source, the summary is in Table 4-6. MAC with cascaded alpha module requires minimum count of component especially switches, on other hand; maximum number of levels. For example, when xMAC-α is composited from three Alpha modules the N_L is 127 levels in 1-DCS configuration, and the total component count are: N_{SW} is 13 switches, N_D is 6 diodes, N_S =3 main sources, and N_{sec}=3 secondary sources

Table 4-7: Summary for xMAC-α$_c$ with first three different added cascaded alpha-cells

Total Alpha Cell Count (N_α)	xMAC-α$_c$					
	N_{SW}	N_D	N_S	N_{sec}	NL in M-DCS	N_L in 1-DCS
2	10	4	2	2	49	31
3	13	6	3	3	249	127
4	16	8	4	4	1249	511

4.3 MAC Topology- Additional Features

In addition to the structural benefits of the MAC topology and its essential role in increasing the number of voltage-levels of the staircase signal that approximates the sinusoidal waveform, MAC has other important features and applications. Among these are symmetric and asymmetric operation configurations, and it's the voltage boosting capability, these features are discussed in this part.

4.3.1 Symmetric and Asymmetric Source Topologies

MAC topology can operate in both symmetric and asymmetric configurations. Symmetric operation configuration is obtained by employing two DC sources topology with equal values or a single dc-source and a capacitor-voltage $V_{sec} = V_{main}$. Asymmetric configuration is obtained with different voltage-reference values. However, the symmetric and asymmetric configurations of the basic topologies affect the maximum number of converter voltage levels and the voltage boosting gain.

For example, the number of levels obtained with the MAC topology of Figure 4-1 is five for the symmetric topology, seven for asymmetric topology with $V_{sec} = \frac{V_{main}}{2}$,, and nine for $V_{sec} = \frac{V_{main}}{3}$,.   Moreover, voltage boosting is higher for the

symmetric basic topology than for the asymmetric one. In fact, the output Voltage

is 2 Vmain for the symmetric versus $\frac{3V_{main}}{2}$ and $\frac{4V_{main}}{3}$ for the asymmetric

configuration with secondary sources of $\frac{V_{main}}{2}$ and $\frac{V_{main}}{3}$, respectively. Figure 4-1

is five for the symmetric topology, seven for asymmetric topology with V_{sec}

$=\frac{V_{main}}{2}$, and nine for $V_{sec} = \frac{V_{main}}{3}$ as shown in Table 4-8.

TABLE 4-8: Specifications of Symmetric and Asymmetric
Features for Basic-MAC Structure

	Symmetrical	Asymmetrical	
		Binary	Ternary
# of Levels	5	7	9
V_{sec}	V_{main}	$\frac{V_{main}}{2}$	$\frac{V_{main}}{3}$
V_{DC} (boost ratio)	2 V_{main}	$\frac{3V_{main}}{2}$	$\frac{4V_{main}}{3}$
Source's ratio configurations	M-DCS	1-DCS	M-DCS & 1-DCS

Another feature of xMAC is 1-DCS configuration can be applied in the same

asymmetric and it's all equations for multiple source instead of single DC-source

and several capacitors, but the number of level (N_L) is lower.

4.3.2 Voltage Boosting

Modular scalability of MAC converter using extra β-cells, Figure 3-9(a) provides

the proposed MAC topology with a voltage-boosting capability. To do this, each

additional cell (N) in the modular sequence of Added-cells should generate a

voltage step that is related to its position. It is clear that voltage-step of a given cell

is half of the preceding one. The output voltage level V_o of the inverter at any time

instant T is obtained by the algebraic sum of the voltage levels of all the activated cells.

The output peak voltage of the extended-topology is constructed by the activation of all the N cells of the modular sequence, it is also depending on the two source count configurations. This peak voltage converges asymptotically to the maximum boosted-voltage ($V_{o,peak}$) values according to M-DCS and 1-DCS configurations of added cell types and modules. The peak output voltage in Basic form: for nine-level MAC (MAC9) is $\frac{4V_{main}}{3}$. And for seven-level MAC7 (1-DCS) is $\frac{3V_{main}}{2}$.

4.3.2.1 Voltage Boosting for Form-I: xMAC-β

MAC in form-I which is presented by different types of beta-cells based on Table 4-2, this part is presented using the two-ratio configuration:

A. M-DCS configuration:

The gain boosting which is increasing with number of added β-cell modules based on Table 3-4:

β_1-module:

$$Vo, peak = \frac{10(2)^{N-1} + 2((2)^{N-1}-1)*V_{main}}{((2)^{N+2}-1)} \tag{4-16}$$

The peak voltage for 1st added Beta-1 in this configuration is $\frac{10V_{main}}{7}$ for MAC21

β_2-module:

$$V_{o,peak} = \frac{(2)^{N+3} - N - 4 * V_{main}}{((2)^{N+2} - 1)}$$

$$\tag{4-17}$$

The peak voltage for 1st added Beta-2 in this configuration is $\frac{11V_{main}}{7}$ for MAC23

β₃-module:

$$V_{o,peak} = \frac{((3^{N+2}-1)/2)*V_{main}}{((3)^{N+1})} \tag{4-18}$$

The peak voltage for 1ˢᵗ added Beta-3 is $\frac{13V_{main}}{9}$ for MAC27.

After adding one, two, or three Beta-1 cells in M-DCS, the voltage gain raises to $\frac{10}{7}$, $\frac{22}{15}$, and $\frac{46}{31}$, respectively. Also, adding the same number of Beta-2 cells and in the same configuration raises the voltage gain raises to $\frac{11}{7}$, $\frac{26}{15}$, and $\frac{57}{31}$, respectively. While adding the same number of Beta-3 cells and in the same configuration raises the voltage gain raises to $\frac{13}{9}$, $\frac{40}{27}$, and $\frac{134}{81}$, respectively.

B. 1-DCS configuration:

According to Table 3-5, the gain boosting for same number of added Beta cells (β₁, β₂, or β₃) is raises $\frac{5}{4}$, $\frac{11}{8}$ and $\frac{23}{16}$ based on the equation:

$$V_{o,peak} = \frac{6(2)^{N-1}-1*V_{main}}{(2)^{N+1}} \tag{4-19}$$

C. 1-DCS configuration for multiple DC-sources:

Where N starts from N=1 in equation (4-4), when 1-DCS configuration characteristics and asymmetric ratio equations are applied for multiple DC-sources, the voltage gain for MAC with added β₁ modules:

$$V_{o,peak} = \frac{6(2)^{N-1} - 1 * V_{main}}{(2)^{N+1}}$$ (4-20)

For example, the voltage gain for MAC with is raises to $\frac{5}{4}$, $\frac{11}{8}$, and $\frac{23}{16}$, respectively.

And for β_2 and β_3 is by:

$$V_{o,peak} = \frac{7(2)^{N-1} + N - 1 * V_{main}}{(2)^{N+1}}$$ (4-21)

For example, the voltage gain for MAC with β_2 and β_3 is raises to $\frac{7}{4}$, $\frac{15}{8}$, and $\frac{31}{16}$, respectively.

4.3.2.2 Voltage Boosting for Form-II: xMAC-α_c

MAC in form-II which is presented by cascaded alpha-modules only based on Table 4-3. this part is presented using the two-ratio configuration:

A. M-DCS configuration, the peak voltage of cascaded alpha of MAC is by:

$$V_{o,\,peak} = \frac{((5)^{\wedge}N_\alpha - 1) * (V_{main,\alpha o})}{15 * 5^{\wedge}(N_\alpha - 2)}$$ (4-22)

Where N_L the total number of output voltage levels in M-DCS

N_α the total number of the Alpha-modules count ($N_\alpha \geq 2$)

After adding extra one, two or three Alpha cells with Multiple DC-source, the voltage gain raises to $\frac{24}{15}$, $\frac{124}{75}$, and $\frac{624}{375}$, respectively.

B. 1-DCS configuration, the peak voltage of cascaded alpha of MAC is by:

$$V_{o,\,peak} = \frac{((4)^{\wedge} N_\alpha - 1)*(V_{main,\alpha o})}{12*4^{\wedge}(N_\alpha - 2)}$$

(4-23)

Where N_α the total number of the Alpha-modules count ($N_\alpha \geq 2$)

After adding extra one, two or three Alpha cells with Multiple DC-source, the voltage gain raises to $\frac{15}{12}$, $\frac{63}{48}$, and $\frac{259}{192}$, respectively.

Voltage gain is different from one added module to others, this feature depends on several parameters; number of voltage-references and their operating configurations, levels count, and module type, Figure 4-1, best voltage gain structure is MAC-β_2 in M-DCS-sources configuration, and worst gain MAC-β in 1-DCS. But MAC-α in 1-DCS configuration requires a single DC-source in each alpha module.
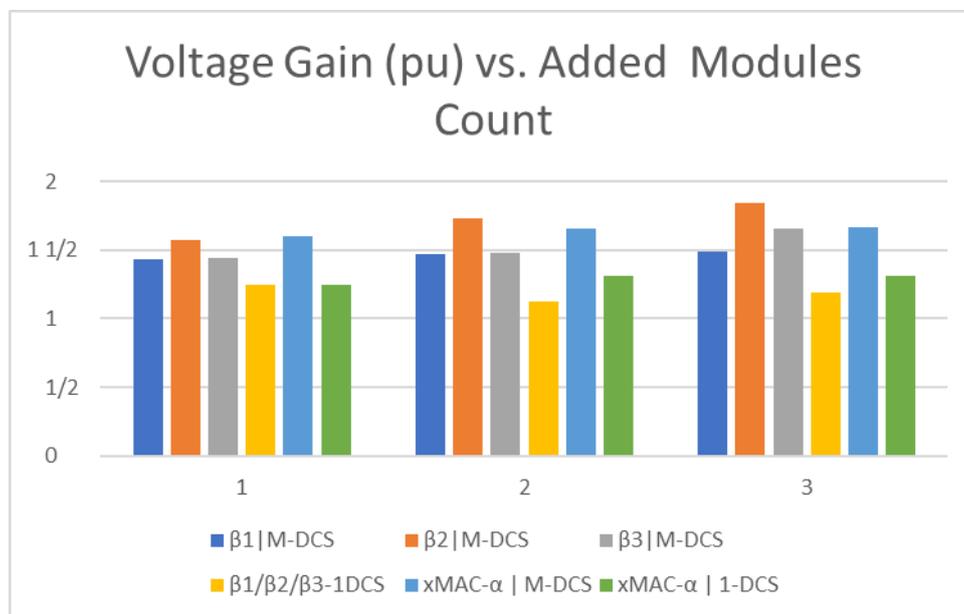
Figure 4-1: Gain verses Added Cells count for xMAC

4.3.3 MAC Verses Other Competitive Topologies

According to [41], the researhers found that most of researchers specify there reviews of MLIs based on several factors such as:

1. Inverter structure and components, e.g. Hybrid/not, single/multiple DC-sources, or CHB included/not. MAC topology is hybrid, works with single/multiple DC-sources, and it includes CHB.

2. Features, e.g. Boosting capability/ Scalibilty/Extended. These three features are in MAC.

3. Inverter Family, e.g. medium-voltage system.

4. Application, e.g. transportation or grid systems integration. MAC could be integrated with grid or not.

Other traditional factors, e.g the level-number (N_L) per switch ratio (LSR), equation:

$$LSR = \frac{N_L}{N_{sw}} \qquad (4\text{-}24)$$

or component per level factor (CLF) to consider among different topologies, high LSR and low CLF circuit is defined as reduced component one, equation:

$$CLF = \frac{All\ component\ count\ without\ filter\ parts}{NL} \qquad (4\text{-}25)$$

These factors aren't enough to give cost ratings of the component into accurate considrations. The number of voltage-references (DC-sources and capacitors) have cost weight in count, ripple of capacitor, and the complexity of control, So a new compartive factor is defined based on voltage-references of MLI's, the level-number per voltage-references ratio (LVR), equation:

$$LVR = \frac{N_L}{N_S + N_C} \qquad\qquad (4\text{-}26)$$

A reduced component count circuit can be found by start with the prioity in comporison by factor LSR then LVR, and then CLF. When LSR is lowest, then the circuit is reduced, if not, LVR is the next factor to compare with, and so on. This comparison is also based on five parameters, to obtain lower switches and sources count, reducing ON switches number in a state,and so total cost. The first and main parameter is power switches count, the second is total number of capacitors per inverter for specific voltage level scheme, and the third value is number of active switches per ON-State, the fourth is extended capability, and the last parameter is voltage gain boosting. MAC configuration has a single DC voltage source, power switches, and dioides. It has reduced components count, especially in case of extended MAC topology, when the voltage level is higher; the components count is possible lower. The comparison is presented based on one or more of last mentioned parameters on three parts; MAC9 (Basic), MAC7 (Basic), and xMAC (Extended).

4.3.3.1   Basic-MAC

A. Single DC-source MAC9 (M-DCS)

In comparison with recently 9-level topologies introduced; Table 4-9 lists the components comparison among different 9-level single DC-source topologies, single DC-source MAC9 (M-DCS) inverter has one of reduced componants topologies; for DSCC vs. PUC9, the MAC is with single DC voltage source, lower power switch, lower gate driver circuits, and a single capacitor, PUC9

require two capacitors. PEC9 has same count of power switch verses MAC9, but it requires single auxiliary DC-link capacitors and a voltage balancing technique using redundant states.

Table 4-9: Existing 9L-MLI's vs proposed MAC comparison depending on components count

9L-MLI's	DC source (N_S)	Capacitor (N_C)	Power Switch (N_{SW})	Diode (N_D)
Asym. CHB	2	0	8	0
DSCC	1	2	9	2
9L-CSD	3	0	7	3
CMLI	2	0	9	0
CSC	1	1	8	0
PUC9	1	2	8	0
PEC9	1	2	7	0
Proposed single DC-source MAC9	1	1	7	2

Other comparison is presented based on previous three factors as illustrated in Table 4-10.

Table 4-10: Existing 9L-MLI's vs proposed MAC in terms of factors comparison

9L-MLI's	LSR	LVR	CLF
Asym. CHB	1.125	4.5	1.112
DSCC	1	3	1.556
9L-CSD	1.286	3	1.445
CMLI	1	4.5	1.223
CSC	1.125	4.5	1.112
PUC9	1.125	3	1.223
PEC9	1.286	3	1.112
Proposed single DC-source MAC9	1.286	4.5	1.223

For verifying this method, the proposed single DC-source MAC9 (M-DCS) and PEC9 are selected as an example to clarify this method, LSR for two inverters are equal, so the next factor to compare is LVR which is higher for MAC9, this

indicates that MAC9 is reduced circuit based on these parameters, and LVR especially. LVR is an impact factor for voltage-references cost in count or in controller.

Table 4-11 shows other parameters to determine more advantages; MAC9 has ability of extendable structure and boosting of output voltage to be $(\frac{4}{3})$ of DC voltage source, also it has three ON switches at each six states of nine states, and two ON switches in zero state, so the total number of ON switches which are required to perform full operation of MAC9 inverter is lower, PUC9 has three ON switches in all states, but it don't have the boosting ability.

In comparison with 9L-CSD with same ON switches number at a state, MAC9 has lower components count.

TABLE 4-11: Comparison between existing 9L-MLI's vs proposed MAC inverter depending on switches count per level and extended option

9L-MLI's	# of Active Switch's per level	Features *, **
Asym. CHB	4	BA, X
DSCC	4	BA, Not X
9L-CSD	Most 3+ Diode	BA, X
CSC-PUC	4	BA, X
CMLI	4	BA, Not X
PUC9	4	Not BA, X
PEC9	3	Not BA, X
Proposed single DC-source MAC9	Most 3+ Diode	BA, X

Boosting Ability (BA) means Output voltage of MLI is bigger than the biggest input DC sources

**X means extendable inverter with using extra cells as topology allows*

B. MAC7 (1-DCS) vs. IPUC7

IPUC7 is a seven-level improved PUC, this derived PUC has worth feature verse the conventional PUC; the voltage boosting capability, but it is more cost due to big count of power switches (nine switches). On other hand; basic-topology of single DC-source MAC7 (1-DCS) staisfies the voltage boosting feature, lower number of power switches (seven switches) for same level number, compatibility for added Beta cells for extended voltage levels with minimized switches count, Table 4-12.

TABLE 4-12: Comparison between proposed MAC inverter vs. IPUC7 in terms of component count, and main parameters

	N_S	N_C	N_{SW}	N_D	BA*	X**
IPUC7	1	1	9	0	√	√ cascaded IPUC7
The proposed MAC7	1	1	7	2	√	√ Multiple Added Cells and reduced components of cascaded concept

Boosting Ability (BA) means Output voltage of MLI is bigger than the biggest input DC sources
**X means extendable inverter with using extra cells as topology allows*

4.3.3.2 Extended-MAC

Extendability is the most compititive feature of MAC-β_1 cell which has the minimum count of switch (one power switch) in 1-DCS configuration, so in each added cell, the switches count increases by one, a capacitor, and a diode. PUC topology is the most compotitive inverter from added cell of single capacitor and two power switches, Figure 4-2 shows comparative analysis for extended MLI using the proposed Extended-MAC with Beta-1 and depending on number of power switches and number of voltage levels and for binary ratio; MAC gives higher levels verses PUC with same number of swiches.
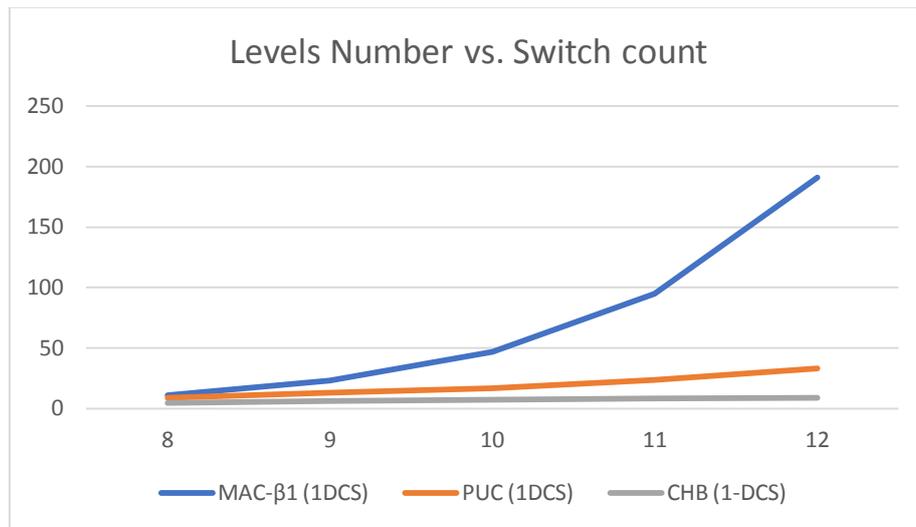
Figure 4-2: Comparative chart between Proposed binary xMAC-β1, PUC, and CHB depending on number of switches, levels, and for single DC-source.

MAC extendable cell includes three types of cells; this gives the flexibility with cost effective for reduced switches and higher level count, MAC's cell are recent mentioned and described, PUC requires two power switches, and a capacitor for each extendable cell and it gives levels count lower than Extended-MAC, Also; Comparison verses PUC cell is worthly using reduced MAC cell; the β_1 which is consist of a single capacitor, one power switch, and a diode, incrementely. And with binary CHB which needs high switch count for same levels.

Boosting ability of MAC is increasing for higher levels structure, and other feature; the proposed inverter required reduced component count and lower number of active switches per ON-state, so power losses of switching and conduction is lower. For example, MAC11-β_1 which has eight switches, single DC-source, three diodes, two capacitors, it generates eleven-levels with voltage gain up to $\frac{7}{4}$ pu. But PUC9 required eight switches to generate nine-levels without voltage boosting

gain feature. The added diodes of MAC11-β_1 gives boosting gain and two levels more than PUC9 in the same asymmetric ratio configuration (1-DCS). These differences are increased with extended cell's structure.

a. MAC11-β_1 vs. PUC9

Extended-topology of MAC with single Beta-1 in 1-DCS configuration staisfy the voltage boosting feature, lower number of power switches (eight switches) for 11-levels, it has the compatibility for added Beta cells for extended voltage levels with minimized switches count. PUC9 has the same number of switches count, capacitors, and sources, but it hasn't voltage boostiong capaibilty, on other hand, MAC11-β1 gives 11 levels with extra three diodes only, and it has highest LSR, Table 4-13.

TABLE 4-13: Comparison between proposed MAC11-β1 inverter vs. PUC9 based on component count, and main parameters

	Ns	Nc	Nsw	N_D	LSR	BA*	X**
PUC9	1	2	8	0	1.125	No	Yes, U-Cell
The proposed MAC11-β₁	1	2	8	3	1.375	Yes	Yes, Multiple Added Cells and reduced components of intersection and cascaded concept

Boosting Ability (BA) means Output voltage of MLI is bigger than the biggest input DC sources

**X means extendable inverter with using extra cells as topology allows*

b. MAC49-α2ₑ vs. 49L-Modified PUC49

The two 49-level topologies operate in M-DCS configuration, the number of output voltage levels and sources count are the same, but the proposed MAC49-2αₑ requires 10 switches; four of them are H-Bridge with modularity states [45]. 49L-Modified PUC49 is shown in Figure 4-3.
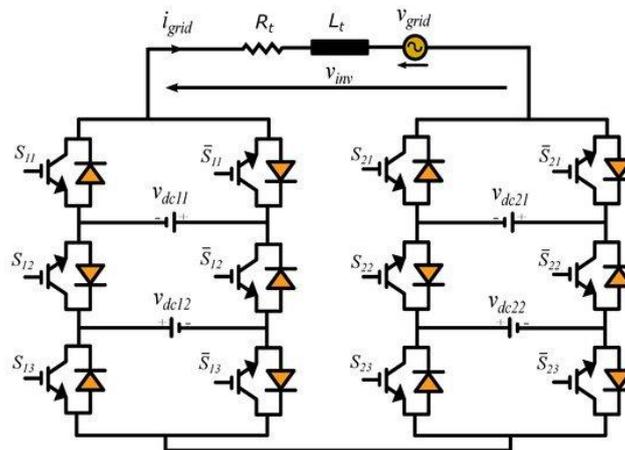
Figure 4-3: Schematic of 49L-Modified PUC [45]

On other hand, the proposed 49-level MAC gives 49 levels based on 10 switches with extra four diodes only, and it has highest LSR, Table 4-14.

TABLE 4-14: Comparison between proposed MAC49-2α$_c$ vs. 49L-MPUC based on component count, and main parameters

	Ns	Nsw	N$_D$	LSR	BA*	X**
49L-MPUC	2	12	0	4.08	Yes	Yes, cascaded PUC5 structure
The proposed MAC49-2α$_c$	2	10	4	4.90	Yes	Yes, Multiple Added Alpha modules and reduced switches of cascaded concept

Boosting Ability (BA) means Output voltage of MLI is bigger than the biggest input DC sources
**X means extendable inverter with using extra cells as topology allows*

Chapter five presents the principle of operation for derivate major structures of the proposed MAC, then the detailed parameters design of these circuits and verifying the forms by applying the proposed control methods for two connections: Standalone and Grid-connected.

CHAPTER 5
MAC DESIGN & CONTROL SYSTEMS

In this chapter, principle of operation and detailed design of mentioned structures of each MAC form; MAC9, MAC-β_1, MAC-β_2, MAC-β_3, and MAC with Cascaded Alpha-cells (MAC-α_c) in M-DCS configuration, also single DC-source MAC9 (M-DCS), MAC7 (1-DCS), and MAC11-β_1 (1-DCS).

Moreover, control method is the most important process in multilevel inverter performance, this method includes the technique that represents the desired states of inverter behavior into gates driving signal of pulses. Multilevel inverter control is depending on several parameters such as number of desired voltage-levels, count of power switches, and the complexity of control system.

Two cases of connections are presented; Standalone and Grid-Connected, each case is applied for a control system of several of MAC topology forms.

1) For Standalone, this case includes two controllers:

   A. it is an open-loop control system based on Multicarrier Sinusoidal Pulse Width Modulation technique (SPWM), this technique is applied on each type of MAC family; MAC9, MAC-β_1, MAC-β_2, MAC-β_3, and MAC with Cascaded Alpha-cells (MAC-α_c)) in M-DCS configuration for verifying MAC purposes.

   B. The proposed control strategy is using Finite Control Set –Predictive Control technique (FCS-MPC), MPC is applied on single DC-source MAC's forms: basic single DC-source MAC9(M-DCS).

2) The second case; the Grid-Connected; the proposed control strategy is using previous FCS-MPC, MPC is applied on single DC-source MAC's forms: basic MAC9(M-DCS)/MAC7(1-DCS), and Extended-MAC: the MAC-β_1

The output power of MAC in this thesis to be designed on 5 KVA with Load of 0.999 Displacement Power Factor without filter to show the developed converter results side excluding the filter enhanced; expect the last case of single DC-source MAC9(M-DCS) in standalone connection, this illustrates how THD values of MAC is very low based on reduced switches and sources count.

5.1 Case I: Standalone based on SPWM technique

SPWM is a popular modulation technique for pulses generation that control switches gates to desired level states. This technique is based on comparison process of two main signal types: carrier signal (V_{cr}) and control signal (V_{cn}) which has critical role to determine the states and its width, V_C is desired to be sine signal, SPWM includes two schemes of control signal, unipolar using two control signals and bipolar which uses single control signal, the bipolar modulation is selected.

The comparison bipolar-SPWM process between V_{cr} and V_{cn} is in two cases; when $V_{cr} > V_{cn}$ the output is zero, and when $V_{cr} < V_{cn}$ the output is one. The desired level states must build a semi sinusoidal form, the relation between number of output voltage level (N_L) and the desired output sine wave is proportional, control signal is preferred to be sine signal. So, more levels and

control sine signal mean more shape close to sine wave, a smaller number of harmonics, and small required filter with easier design.

SPWM indices are determinations of this process, the first one is Modulation Index (M_a) which is the relation between amplitude peak value of V_{cr} and value of V_{cn} signals. The most effective scheme of SPWM is level-shift carriers' modulation, in this scheme; the carrier signals are vertically arrangement, level-shift SPWM has three different carrier signal start point, as illustrated in Table 5-1.

Table 5-1: LS-SPWM implementation type [46]

LS-SPWM implementation type	Description
In-phase disposition (IPD)	All carriers are in phase
Alternative phase opposite disposition (APOD)	All carriers are alternatively in opposite disposition
Phase opposite disposition (POD)	The carriers above zero are in phase and which are below zero are in opposition

In this thesis LS-SPWM is employed for proposed MAC structures verifying regarding to its advantages, a single sine waveform (bipolar type) with modulation index of M_a value, and it is assumed to be unity in this thesis, and number of carriers (N_{cr}). N_{cr} is equal (N_L -1) for $N_L \geq 3$ [47].

According to [25] Four carriers of LS-SPWM technique are presented. To use this technique in general for N_{cr}, Figure 5-1 and Figure 5-2 based on this technique show the generalized block diagram and schematic of digital states generation for N_{cr}, respectively.
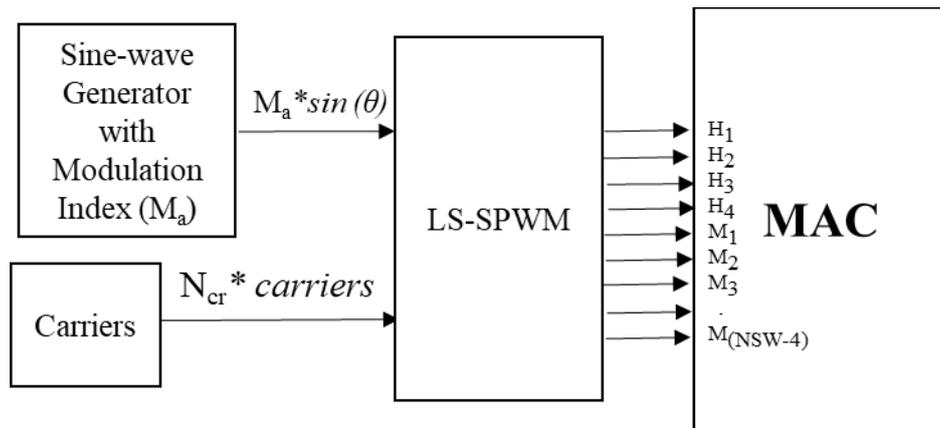
Figure 5-1: Proposed generalized control diagram of LS-SPWM technique for MAC inverter

For LS-PWM block has multiple comparators, each one compares the control signal with the recent level's carrier signal to determine the desired level and then AND Gate with NOT to ensure correct comparison between two levels. Each carrier has gain $K_{cr, gain}$ with level-shift of half-gain as illustrated in Figure 5-2. The outputs are the firing gate pulses of MAC.
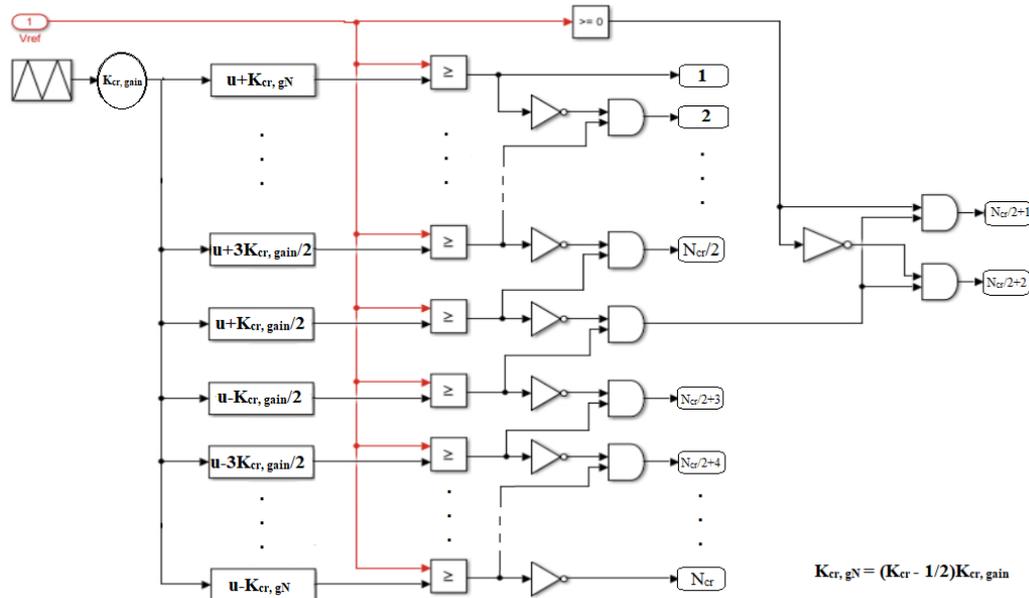
Figure 5-2: Proposed generalized LS-SPWM technique scheme for MAC inverter [25]

In Figure 5-2, the proposed output signal of LS-SPWM scheme from (1 to Ncr) determine the desired state for each MAC's components in Voltage levels generation by MAC activation sequences table. For example, signal 1 refers to state 1 and firing the proposed switches based on Table 5-2, signal 2 to state 2, and so on.

5.1.1 Nine-level MAC (MAC9)

Table 5-2 illustrates the output states for α-module of MAC9. State 2R is the redundant of V_{main} level and it isn't used as main state in the operation sequence due to required two switches for this level.

All-positive half cycle states of Alpha module are (Figure 5-3 (a)) which are using single/multiple DC-Sources:

- State 1: M_2 and M_3 are on, all other switches and diodes are off, this state gives positive $V_{main} + V_{sec}$ level. In this state, the capacitor is discharged (in single DC-source case).

- State 2: M_2 and D_2 are on, all other switches and diodes are off, this state gives $+V_{main}$ level.

- State 3: M_1 and D_2 are on, all other switches and diodes are off, this state gives positive $V_{main} - V_{sec}$ level. In this state, the capacitor is charged (in single DC-source case).

- State 4: M_3 and D_1 are on, all other switches and diodes are off, this state gives $+V_{sec}$ level. In this state, the capacitor is also discharged (in single DC-source case).

The Alpha module output voltage (V_{ab} or $V_{O,\ \alpha}$) activation sequences are illustrated in Table 3-1. The whole output voltage of Basic-MAC (V_{inv}, or V_o) and H-bridge activation sequences in Table 5-2. The activation sequences and the conduction paths of the positive half cycle, zero levels, and the direction of current are shown in Figure 5-3 (a) and (b), respectively. The voltage values of the negative cycle can be directly deduced from the complementary operation of H_1, H_4 and H_2, H_3. States 5 and the redundant 5R are representing the zero-voltage states and the other ten states are providing suitable voltage levels across the V_{ab} voltage which include two redundancy states of (V_{main} and $-V_{main}$).

Table 5-2: Voltage levels generation by MAC9 activation sequences (R: redundant)

MAC9 States & Redundancies	H1, H4	H2, H3	Level Value	V_{ab}	C * For single DC-source
1	1	0	4E	$V_{main} + V_{sec}$	D
2	1	0	3E	V_{main}	B
2R	1	0	3E	V_{main}	B
3	1	0	2E	$V_{main} - V_{sec}$	C
4	1	0	E	V_{sec}	D
5	(1,0)	(1,0)	0	0	B
5R	(1,0)	(1,0)	0	0	B
6	0	1	-E	$- V_{sec}$	D
7	0	1	-2E	$- (V_{main} - V_{sec})$	C
8	0	1	-3E	$- V_{main}$	B
8R	0	1	-3E	$- V_{main}$	B
9	0	1	-4E	$- (V_{main} + V_{sec})$	D

* B/C/D: Bypass, charging, and discharging processes of single DC-source MAC's capacitor

The negative cycle operating is also generated by Gamma-module which is H-bridge simply, this module has H_1 and H_2 in ON-States for positive half cycle and OFF states in case of negative half cycle, where H_3 and H_4 are the complementary of (H_1 and H_2), but in the two zeros states; the pair H_1 and H_3 are ON or pair H_2

and H_4 are ON, the current is reversed and it flows through antiparallel diodes of switches for the same path.

The capacitor charging states are 3 and 7, and its discharging states are 1 and 9, the voltage balancing technique can allow to keep capacitor level within accepted range to be about one third of DC voltage source value that complete the equal voltage staircase (M-DCS ratio). States 5, 5R are the two zero schemes, and there isn't action on capacitor, Figure 5-3 (b). The conduction paths that generate the voltage levels of Table 5-2 are shown in Figure 5-3 for the positive-cycle and zero levels. The negative-cycle voltage levels can be obtained by the complementary operation of the H-bridge as in the Basic-MAC.
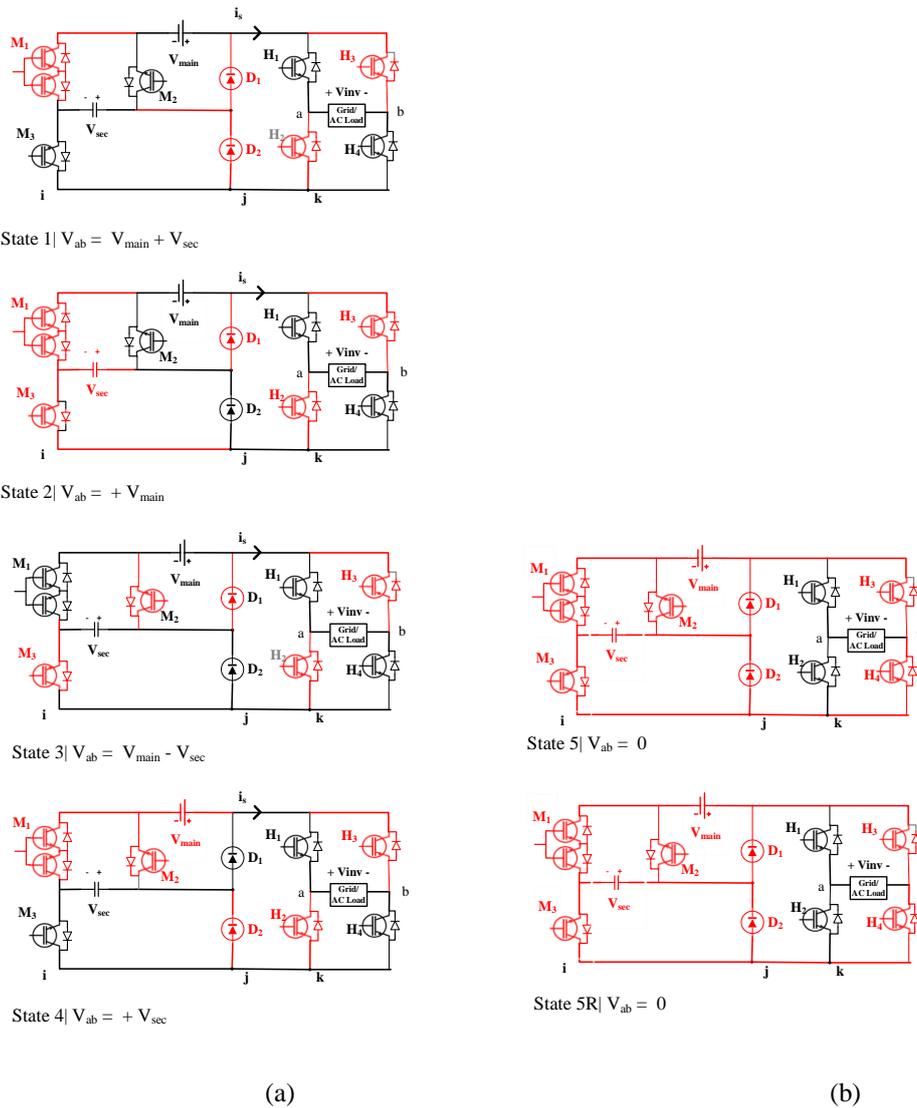
Figure 5-3: The operating states of the proposed MAC9 topology: (a) Positive half cycle states. (b) Zero states

All possible states for MAC9 are also shown in Table 5-2. The operation sequence of the proposed multilevel inverter is (V_{main} + V_{sec}, V_{main}, V_{main} − V_{sec}, V_{sec}, 0, -V_{sec}, - (V_{main} − V_{sec}), V_{main}, -(V_{main} + V_{sec})) in the single-phase topology, this sequence is in a typical waveform of MAC9 output voltage is illustrated in Figure 5-4. Voltage levels can be presented in 9 voltage levels (0, ±E, ±2E, ±3E, ±4E), where E= $\frac{V_{main}}{3}$ which is the voltage reference of each level, the nominal

voltage for the V_{main} is equal to 3E, $V_{sec} = E$. Also, MAC9 is worked with single DC-source in this configuration.
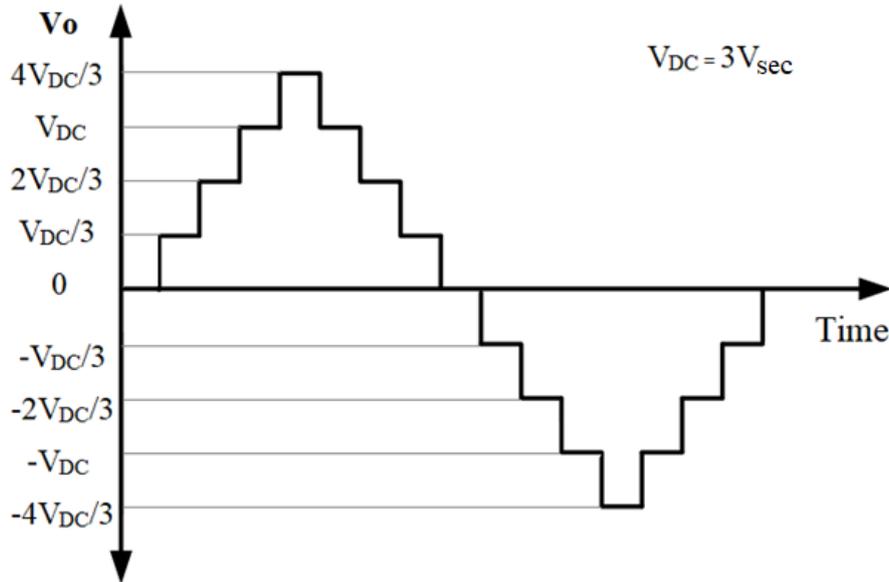
Figure 5-4: Typical waveform of MAC9 in output voltage (Vo=V$_{ab}$), where V$_{main}$=V$_{DC}$

5.1.2 Seven-level MAC (MAC7)

Four-level output states of α-module of MAC7. State 2R is the redundant of V_{main} level and it isn't used as main state in the operation sequence due to required two active switches for this level.

In Table 3-1, the all-positive half cycle states of alpha-module are (Figure 5-6 (a)) which are seven-level in single/multiple DC-sources (instead of the capacitor which doesn't need redundant states), States of MAC7 is the same of previous MAC9, but the voltage-references are with 1-DCS ratio (2:1), it means the V_{main} is twice of V_{sec}. for this configuration; the state 4 in MAC9 is a redundant state in MAC7 for $+V_{sec}$ value.

The inverter output voltage (V_{ab} or V_{inv}) and H-bridge activation sequences are illustrated in Table 5-2. The activation sequences and the conduction paths of the

positive half cycle and zero levels are shown in Figure 5-5 (a) and (b), respectively. The voltage values of the negative cycle can be directly deduced from the complementary operation of H_1, H_4 and H_2, H_3. States 5 and the redundant 5R are representing the zero-voltage states and the other ten states are providing suitable voltage levels across the V_{ab} voltage which include two redundancy states of (V_{main} and -V_{main}).

The negative cycle operating is also generated by Gamma-module which is H-bridge simply, this module has H_1 and H_2 in ON-States for positive half cycle and OFF states in case of negative half cycle, where H_3 and H_4 are the complementary of (H_1 and H_2), but in the two zeros states; the pair H_1 and H_3 are ON or pair H_2 and H_4 are ON, and the current is reversed and it flows through antiparallel diodes of switches for the same path.

Voltage levels can be presented in 7 voltage levels (0, ±E, ±2E, ±3E), where E= $\frac{V_{main}}{2}$ which is the voltage reference of each level, the nominal voltage for the V_{main} is equal to 2E, V_{sec} =E.

The capacitor charging states are 3 and 7, and its charging states are 1 and 9, the voltage balancing technique can allow to keep capacitor level within accepted range to be about one third of DC voltage source value that complete the equal voltage staircase. State 5 and 5R are the two zero schemes, and there isn't action on capacitor, Figure 5-5 (b).

State 1| $V_{ab} = V_{main} + V_{sec}$

State 2| $V_{ab} = + V_{main}$

State 3| $V_{ab} = V_{main} - V_{sec}$

State 4| $V_{ab} = 0$

State 4R| $V_{ab} = 0$

(a)   (b)
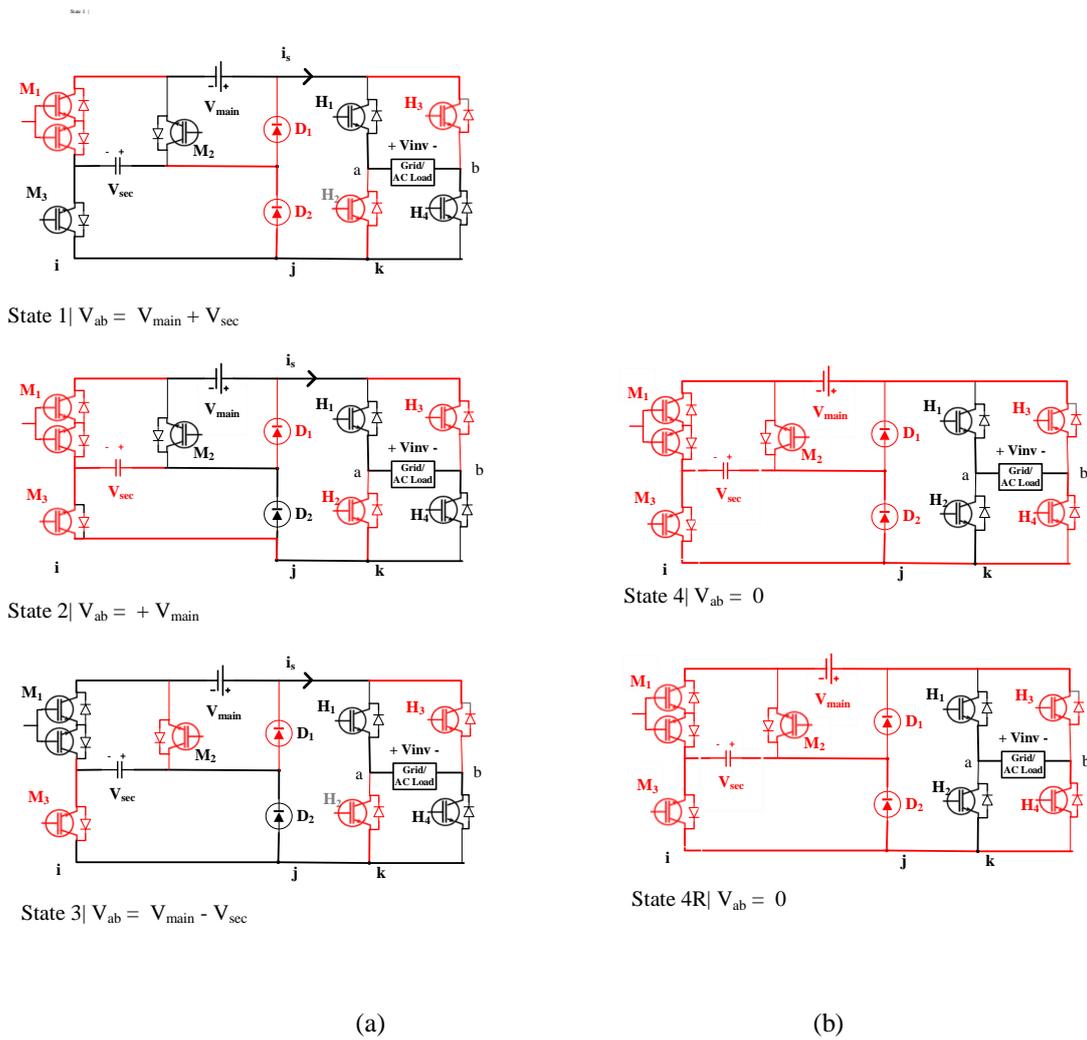
Figure 5-5. The operating states of the proposed MAC7 topology: a) Positive half cycle states. B) Zero states

All possible states are also shown in Table 5-2. The operation sequence of the proposed multilevel inverter is ($V_{main} + V_{sec}$, V_{main}, $V_{main} - V_{sec}$, V_{sec}, 0, -V_{sec}, -($V_{main} - V_{sec}$), V_{main}, -($V_{main} + V_{sec}$)) in the single-phase topology, but the voltage ratio (V_{main}:V_{sec}) is (2:1). This sequence is in a typical waveform of MAC7 output voltage is illustrated in Figure 5-6.
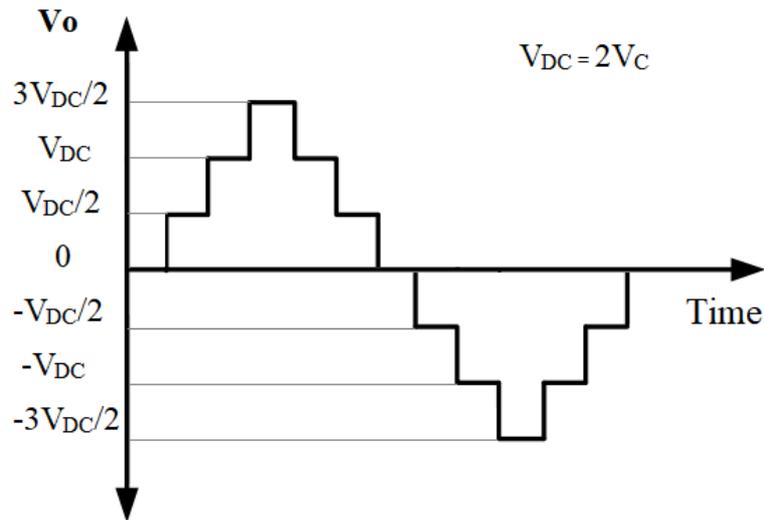
Figure 5-6: Typical waveform of MAC7 output voltage (Vo=V$_{ab}$), where V$_{main}$=V$_{DC}$

In summary, Basic-MAC can work using two different voltage sources ratio:1-DCS ratio (2:1) gives seven-level output, and M-DCS ratio (3:1) generates nine-level outputs, it also works for single/multiple DC-sources.

For MAC9 and MAC7, the digital scheme in Figure 5-7 refers to eight carrier with $\frac{1}{8}$ gain for each carrier with level-shift of $\frac{1}{16}$.
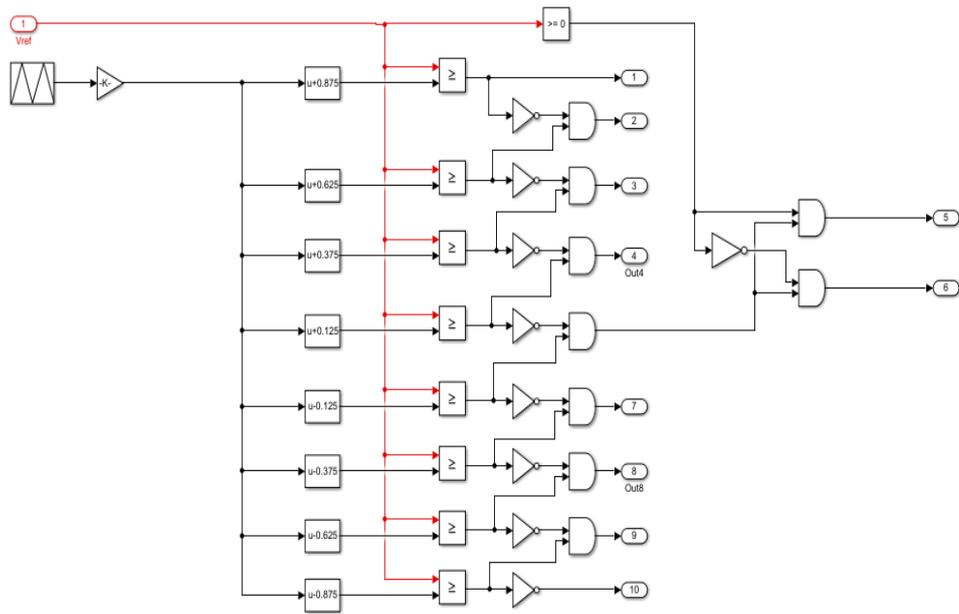
Figure 5-7: Proposed LS-SPWM technique scheme for MAC7 and MAC9 inverters

The LS-SPWM eight carriers and sine control signals for MAC9 are shown in Figure 5-8.
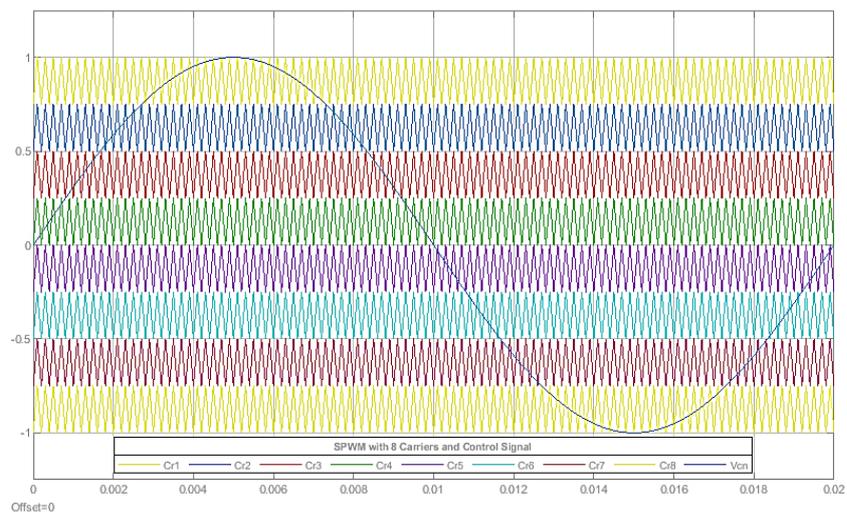
Figure 5-8: LS-SPWM technique output with eight carriers for nine-level inverter

Several Standalone MAC structures are presented in M-DC configuration, the control strategy is open-loop based on bipolar LS-SPWM, the design of each one is found in detail. Major parameters of all designs are listed in Table 5-3.

Table 5-3: Major Parameters for open-loop MAC system

Parameter	Value
$V_{ab, peak}$	311 volts
V_{rms}	220 volts
Fundamental frequency (f_o)	50 Hz
Switching frequency (f_{sw})	2050Hz
Displacement Power Factor (DPF)	0.999

MAC9 is introduced in chapter four, MAC9 structure is consist of two modules; alpha and gamma, Figure 4-1. Nine-level MAC is presented for multiple DC-sources, MAC9 control based on multicarrier SPWM technique requires eight level-shifted carriers (N_{cr}), Table 5-4.

Table 5-4: SPWM Parameters for open-loop MAC9 system

Parameter	Value
V_{main}	3*311/4
V_{sec0}	311/4
Carrier number (N_{cr})	8
$K_{cr, gain}$	¼

5.1.3 MAC21-β_1

MAC-β1 structure is composed of three modules; alpha, single beta-1, and gamma, 21-level MAC is presented in M-DC configuration. MAC with single β1 in M-DCS configuration Operation, in this configuration; all secondary voltage-references (V_{sec0} and V_{sec1}) are DC-sources, Figure 5-9.
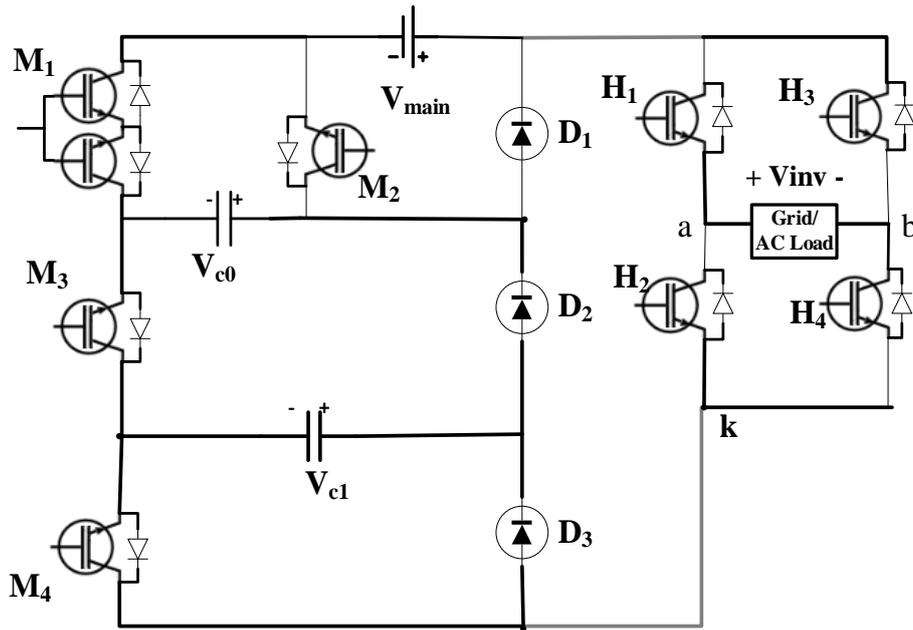
Figure 5-9: Schematic of MAC21-β_1 inverter

All possible states for M-DCS configuration are also shown in Table 5-5 in the same principle.

The positive half-cycle operation sequence of the proposed single-phase multilevel inverter is ($V_{main} + V_{sec0}$, $V_{main} + V_{sec0} - V_{sec1}$, $V_{main} + V_{sec1}$, V_{main}, $V_{main} - V_{sec1}$, $V_{main} - V_{sec0} + V_{sec1}$, $V_{main} - V_{sec0}$, V_{sec0}, $V_{sec0} - V_{sec1}$, V_{sec1}, 0) without mentioning the negative half-cycle sequence due to gamma-module complementary concept.

Voltage levels can be presented on other way; 21 voltage levels (0, $\pm E$, $\pm 2E$, $\pm 3E$, $\pm 4E$, $\pm 5E$, $\pm 6E$, $7E$, $\pm 8E$, $\pm 9E$, $\pm 10E$), where E= $\frac{V_{main}}{7}$ which is the voltage reference of each level, the nominal voltage for the V_{main} is equal to 7E, $V_{sec0} = 3E$, and $V_{sec1} = E$.

Table 5-5: Zero and positive half-cycle voltage levels generation by MAC21-β_1 activation sequences (without redundancies)

State	Output Level (V_o)	Level Value	M_1	M_2	M_3	M4	D_1	D_2	D_3	(H1, H4), (H2, H3)
1	$V_{main} + V_{sec0}$	10E	0	1	1	1	Off	Off	Off	(0,0), (1,1)
2	$V_{main} + V_{sec0} - V_{sec1}$	9E	0	1	1	0	Off	Off	On	(0,0), (1,1)
3	$V_{main} + V_{sec1}$	8E	0	1	0	1	Off	On	Off	(0,0), (1,1)
4	V_{main}	7E	0	1	0	0	Off	On	On	(0,0), (1,1)
5	$V_{main} - V_{sec1}$	6E	1	0	1	0	Off	Off	On	(0,0), (1,1)
6	$V_{main} - V_{sec0} + V_{sec1}$	5E	1	0	0	1	Off	On	Off	(0,0), (1,1)
7	$V_{main} - V_{sec0}$	4E	1	0	0	0	Off	On	On	(0,0), (1,1)
8	V_{sec0}	3E	0	0	1	1	On	Off	On	(0,0), (1,1)
9	$V_{sec0} - V_{sec1}$	2E	0	0	1	0	On	Off	On	(0,0), (1,1)
10	V_{sec1}	E	0	0	0	1	On	On	Off	(0,0), (1,1)
11	0	0	0	0	0	0	Off	Off	Off	(1,0), (1,0)
11R	0	0	0	0	0	0	Off	Off	Off	(0,1), (0,1)

MAC21-β_1 control based on multicarrier SPWM technique requires 20 level-shifted carriers (N_{cr}), parameters are listed Table 5-6.

Table 5-6: SPWM Parameters for open-loop MAC21-β_1 system

Parameter		Value
Alpha	V_{main}	7*311/10
	V_{sec0}	3*311/10
Beta-1	V_{sec1}	1*311/10
Carriers count and gain	**Carrier number (N_{cr})**	20
	$K_{cr, gain}$	1/10

5.1.4 MAC23-β_2

MAC-β_2 structure is composed of three modules; alpha, single beta-2, and gamma, 23-level MAC is presented in M-DCS configuration, Figure 5-10.
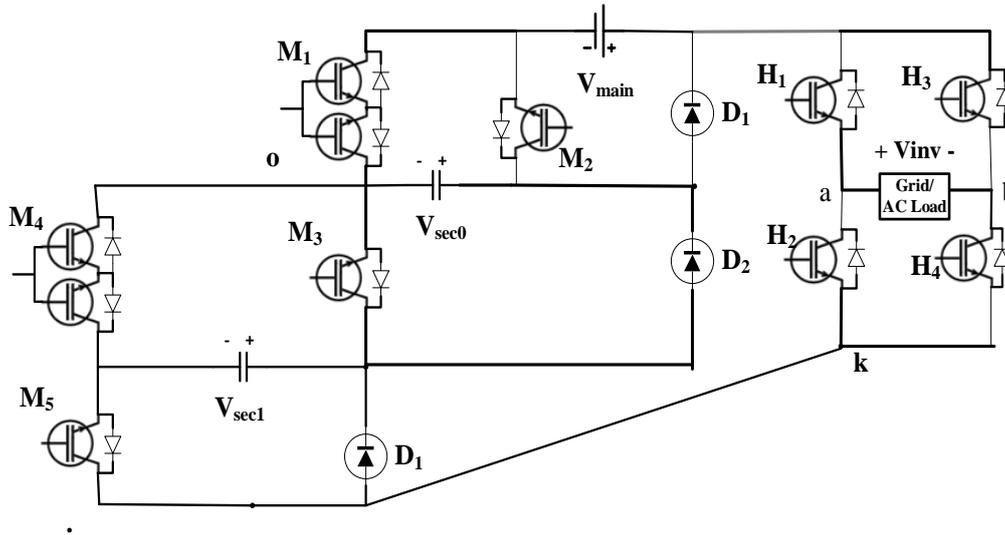
Figure 5-10: Schematic of MAC23-β2 inverter

All possible states for M-DCS configuration are also shown in Table 5-7 in the same principle.

The positive half-cycle operation sequence of the proposed single-phase multilevel inverter is without mentioning the negative half-cycle sequence due to gamma-module complementary concept.

Voltage levels can be presented in 23 voltage levels (0, $\pm E$, $\pm 2E$, $\pm 3E$, $\pm 4E$, $\pm 5E$, $\pm 6E$, $\pm 7E$, $\pm 8E$, $\pm 9E$, $\pm 10E$, $\pm 11E$), where $E = \frac{V_{main}}{7}$ which is the voltage reference of each level, the nominal voltage for the V_{main} is equal to $7E$, $V_{sec0} = 3E$, and $V_{sec1} = E$.

Table 5-7: Zero and positive half-cycle voltage levels generation by MAC23-β_2 activation sequences (without redundancies)

St.	Output Level (V_o)	Level Value	M_1	M_2	M_3	M_4	M_5	D_1	D_2	D_3	(H1, H4), (H2, H3)
1	$V_{main} + V_{sec0} + V_{sec1}$	11E	0	1	1	1	1	Off	Off	Off	(0,0), (1,1)
2	$V_{main} + V_{sec0}$	10E	0	1	1	1	0	Off	Off	On	(0,0), (1,1)
3	$V_{main} + V_{sec0} - V_{sec1}$	9E	0	1	1	0	0	Off	Off	Off	(0,0), (1,1)
4	$V_{main} + V_{sec1}$	8E	0	1	0	1	1	Off	Off	On	(0,0), (1,1)
5	V_{main}	7E	0	1	0	1	0	Off	On	On	(0,0), (1,1)
6	$V_{main} - V_{sec1}$	6E	0	1	0	0	0	Off	On	On	(0,0), (1,1)
7	$V_{main} - V_{sec0} + V_{sec1}$	5E	1	0	0	1	1	Off	On	Off	(0,0), (1,1)
8	$V_{sec0} + V_{sec1}$	4E	0	0	1	1	1	On	Off	Off	(0,0), (1,1)
9	V_{sec0}	3E	0	0	1	1	0	On	Off	On	(0,0), (1,1)
10	$V_{sec0} - V_{sec1}$	2E	0	0	1	0	0	On	Off	On	(0,0), (1,1)
11	V_{sec1}	E	0	0	0	1	1	On	On	Off	(0,0), (1,1)
12	0	0	0	0	0	0		Off	Off	Off	(1,0), (1,0)
12R	0	0	0	0	0	0		Off	Off	Off	(0,1), (0,1)

MAC23-β_2 control based on multicarrier SPWM technique requires 22 level-shifted carriers (N_{cr}), Table 5-8.

Table 5-8: SPWM Parameters for open-loop MAC23-β_2 system

Parameter		Value
Alpha	V_{main}	$\dfrac{7 * 311}{11}$
	V_{sec0}	$\dfrac{3 * 311}{11}$
Beta-2	V_{sec1}	$\dfrac{311}{11}$
Carriers count and gain	Carrier number (N_{cr})	22
	$K_{cr, gain}$	$\dfrac{1}{11}$

5.1.5 MAC27-β_3

MAC-$\beta3$ structure is composed of three modules; alpha, single beta-3, and gamma, 27-level MAC is presented in M-DCS configuration, Figure 5-11.
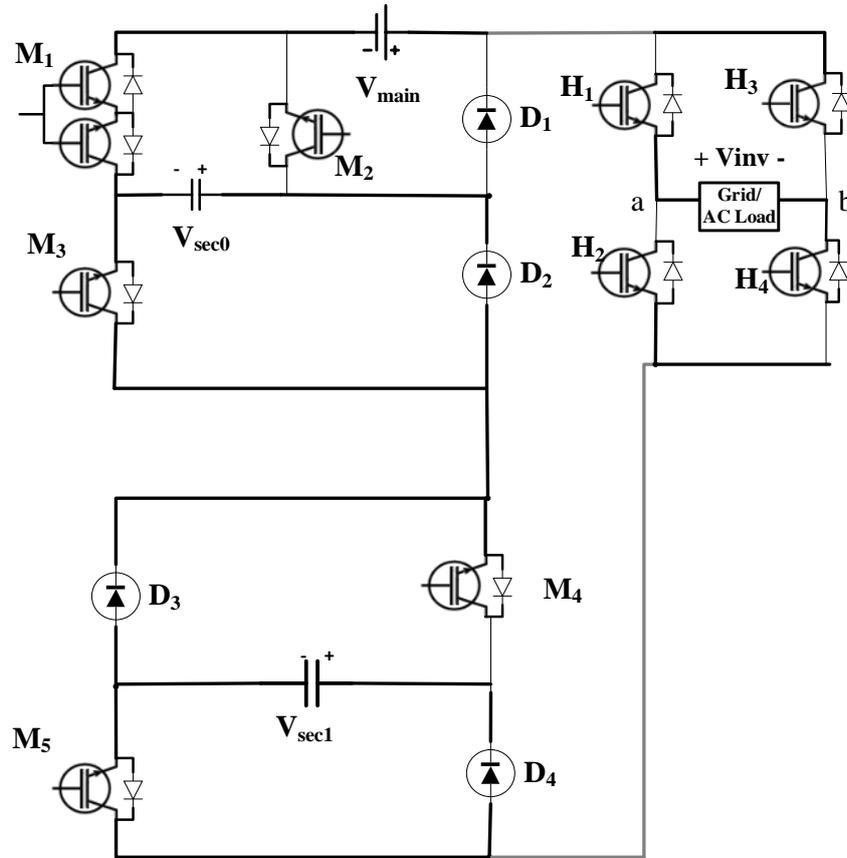
Figure 5-11: Schematic of MAC27-β_3 inverter

All possible states for M-DCS configuration are also shown in Table 5-9 in the same principle.

The positive half-cycle operation sequence of the proposed single-phase multilevel inverter is without mentioning the negative half-cycle sequence due to gamma-module complementary concept.

Voltage levels can be presented in 27 voltage levels (0, $\pm E$, $\pm 2E$, $\pm 3E$, $\pm 4E$, $\pm 5E$, $\pm 6E$, $\pm 7E$, $\pm 8E$, $\pm 9E$, $\pm 10E$, $\pm 11E$, $\pm 12E$, $\pm 13E$), where $E = \frac{V_{main}}{9}$ which is the voltage reference of each level, the nominal voltage for the V_{main} is equal to 9E, $V_{sec0} = 3E$, and $V_{sec1} = E$.

Table 5-9: Zero and positive half-cycle voltage levels generation by MAC27-β₃ activation

sequences (without redundancies)

St.	Output Level (V_o)	Level Value	M_1	M_2	M_3	M_4	M_5	D_1	D_2	D_3	D_4	(H1, H4), (H2, H3)
1	$V_{main} + V_{sec0} + V_{sec1}$	13E	0	1	1	1	1	Off	Off	Off	Off	(0,0), (1,1)
2	$V_{main} + V_{sec0}$	12E	0	1	1	1	0	Off	Off	Off	On	(0,0), (1,1)
3	$V_{main} + V_{sec0} - V_{sec1}$	11E	0	1	1	0	0	Off	Off	On	On	(0,0), (1,1)
4	$V_{main} + V_{sec1}$	10E	0	1	0	1	1	Off	On	Off	Off	(0,0), (1,1)
5	V_{main}	9E	0	1	0	1	0	Off	On	Off	On	(0,0), (1,1)
6	$V_{main} - V_{sec1}$	8E	0	1	0	0	0	Off	On	On	On	(0,0), (1,1)
7	$V_{main} - V_{sec0} + V_{sec1}$	7E	1	0	0	1	1	Off	On	Off	Off	(0,0), (1,1)
8	$V_{main} - V_{sec0}$	6E	1	0	1	1	0	Off	On	Off	On	(0,0), (1,1)
9	$V_{main} - V_{sec0} - V_{sec1}$	5E	1	0	0	0	0	Off	On	On	On	(0,0), (1,1)
10	$V_{sec0} + V_{sec1}$	4E	0	0	1	1	1	On	Off	Off	Off	(0,0), (1,1)
11	V_{sec0}	3E	0	0	1	1	0	On	Off	Off	On	(0,0), (1,1)
12	$V_{sec0} - V_{sec1}$	2E	0	0	1	0	0	On	Off	On	On	(0,0), (1,1)
13	V_{sec1}	E	0	0	0	1	1	On	On	Off	Off	(0,0), (1,1)
14	0	0	0	0	0	0		Off	Off	Off	Off	(1,0), (1,0)
14R	0	0	0	0	0	0		Off	Off	Off	Off	(0,1), (0,1)

MAC27-β₃ control based on multicarrier SPWM technique requires 26 level-shifted carriers (N_{cr}), Table 5-10.

Table 5-10: SPWM Parameters for open-loop MAC27-β₃ system

Parameter		Value
Alpha	V_{main}	$\dfrac{9*113}{13}$
	V_{sec0}	$\dfrac{3*311}{13}$
Beta-3	V_{sec1}	$\dfrac{311}{13}$
Carriers count and gain	**Carrier number (N_{cr})**	26
	$K_{cr, gain}$	$\dfrac{1}{13}$

5.1.6 MAC49-2α$_c$

MAC-α structure is consisting of three modules; cascaded alpha and gamma, 49-level MAC is presented in M-DC configuration, Figure 5-12.
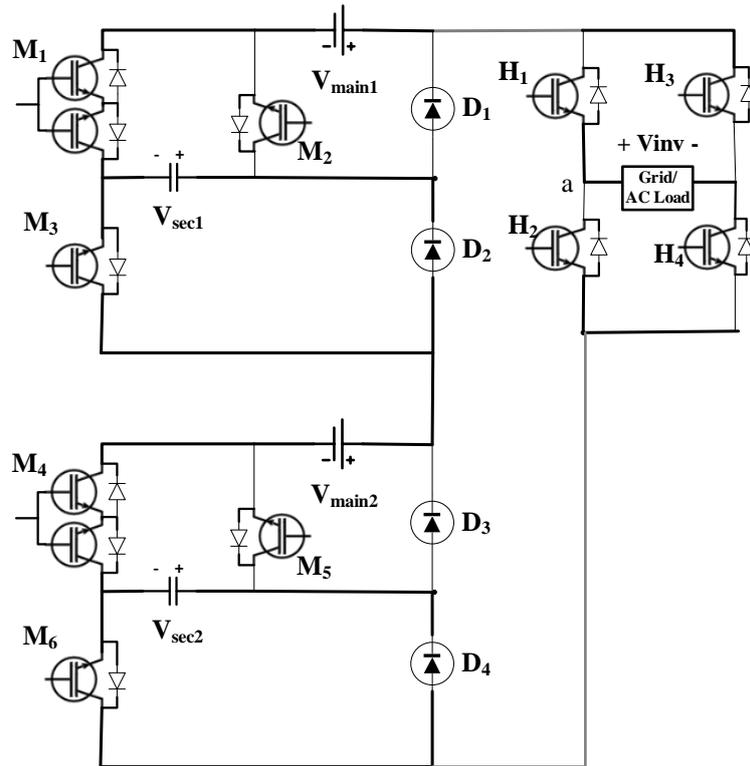
Figure 5-12: MAC-2αc inverter

All possible states for M-DCS configuration are also shown in Table 5-11 in the same principle.

The positive half-cycle operation sequence of the proposed single-phase multilevel inverter is without mentioning the negative half-cycle sequence due to gamma-module complementary concept.

Voltage levels can be presented in 45 voltage levels (0, $\pm$E, $\pm$2E, $\pm$3E, $\pm$4E, $\pm$5E, $\pm$6E, $\pm$7E, $\pm$8E, $\pm$9E, $\pm$10E, $\pm$11E, $\pm$12E, $\pm$13E, $\pm$14E, $\pm$15E, $\pm$16E, $\pm$17E, $\pm$18E, $\pm$19E, $\pm$20E, $\pm$21E, $\pm$22E, $\pm$23E, $\pm$24E), where E= $\frac{V_{main}}{15}$ which is the voltage reference of each level, the nominal voltage for the V_{main0} is equal to 15E, $V_{sec0} = $5E, V_{main1} = 4E and $V_{sec1} = $E.

Table 5-11: Zero and positive half-cycle voltage levels generation by MAC45-2α_c activation sequences (without redundancies)

St.	Output Level (V_o)	Level value	M_1	M_2	M_3	M_4	M_5	M_6	D_1	D_2	D_3	D_4	(H1, H4), (H2, H3)
1	$V_{main0} + V_{sec0} + V_{main1} + V_{sec1}$	24E	0	1	1	0	1	1	Off	Off	Off	Off	(0,0), (1,1)
2	$V_{main0} - V_{sec0} + V_{main1}$	23E	0	1	1	1	1	0	Off	Off	Off	On	(0,0), (1,1)
3	$V_{main0} + V_{sec0} + V_{main1} - V_{sec1}$	22E	0	1	1	1	0	0	Off	Off	Off	On	(0,0), (1,1)
4	$V_{main0} + V_{sec0} + V_{sec1}$	21E	0	1	1	0	0	1	Off	Off	On	Off	(0,0), (1,1)
5	$V_{main0} + V_{sec0}$	20E	0	1	1	0	0	0	Off	Off	On	On	(0,0), (1,1)
6	$V_{main0} + V_{main1} + V_{sec1}$	19E	0	1	0	0	1	1	Off	On	Off	Off	(0,0), (1,1)
7	$V_{main0} + V_{main1}$	18E	0	1	0	0	1	0	Off	On	Off	On	(0,0), (1,1)
8	$V_{main0} + V_{main1} - V_{sec1}$	17E	0	1	0	1	0	0	Off	On	Off	On	(0,0), (1,1)
9	$V_{main0} + V_{sec1}$	16E	0	1	0	0	0	1	Off	On	On	Off	(0,0), (1,1)
10	V_{main0}	15E	0	1	0	0	0	0	Off	On	On	On	(0,0), (1,1)
11	$V_{main0} - V_{sec0} + V_{main1} + V_{sec1}$	14E	1	0	0	0	1	1	Off	On	Off	Off	(0,0), (1,1)
12	$V_{main0} - V_{sec0} + V_{main1}$	13E	1	0	0	0	1	0	Off	On	Off	On	(0,0), (1,1)
13	$V_{main0} - V_{sec0} + V_{main1} - V_{sec1}$	12E	1	0	0	1	0	0	Off	On	Off	On	(0,0), (1,1)
14	$V_{main0} - V_{sec0} + V_{sec1}$	11E	1	0	0	0	0	1	Off	On	On	Off	(0,0), (1,1)
15	$V_{main0} - V_{sec0}$	10E	1	0	0	0	0	0	Off	On	On	On	(0,0), (1,1)
16	$V_{sec0} + V_{main1} + V_{sec1}$	9E	0	0	1	0	1	1	On	Off	Off	Off	(0,0), (1,1)
17	$V_{sec0} + V_{main1}$	8E	0	0	1	0	1	0	On	Off	Off	On	(0,0), (1,1)
18	$V_{sec0} + V_{main1} - V_{sec1}$	7E	0	0	1	1	0	0	On	Off	Off	On	(0,0), (1,1)
19	$V_{sec0} + V_{sec1}$	6E	0	0	1	0	0	1	On	Off	On	Off	(0,0), (1,1)
20	V_{sec0}	5E	0	0	1	0	0	0	On	Off	On	On	(0,0), (1,1)
21	$V_{main1} + V_{sec1}$	4E	0	0	0	0	1	1	On	On	Off	Off	(0,0), (1,1)
22	V_{main1}	3E	0	0	0	0	1	0	On	On	Off	On	(0,0), (1,1)
23	$V_{main1} - V_{sec1}$	2E	0	0	0	1	0	0	On	On	Off	On	(0,0), (1,1)
24	V_{sec1}	E	0	0	0	0	0	1	On	On	On	Off	(0,0), (1,1)
25	0	0	0	0	0	0	0	0	Off	Off	Off	Off	(1,0), (1,0)
25R	0	0	0	0	0	0	0	0	Off	Off	Off	Off	(0,1), (0,1)

MAC49-2αc control based on multicarrier LS-SPWM technique requires 48

level-shifted carriers (N_{cr}), Table 5-12.

Table 5-12: SPWM Parameters for open-loop MAC49-2αc system

Parameter		Value
1st Alpha	**V_{main1}**	$\dfrac{9 * 311}{13}$
	V_{sec1}	$\dfrac{3 * 311}{13}$
2nd Alpha	**V_{main2}**	$\dfrac{4 * V_{sec1}}{5}$
	V_{sec2}	$\dfrac{V_{sec1}}{5}$
Carriers count and gain	**Carrier number (N_{cr})**	48
	$K_{cr, gain}$	$\dfrac{1}{24}$

5.2 Case II: Grid-Connected based on FCS-MPC

The conventional FCS-MPC control technique is selected to get direct validation proposed inverter by grid-current tracking while keeping the capacitors voltage at its nominal value. This technique is applied on several MAC forms in closed-control strategy.

5.2.1 Grid Model

The Model of grid is voltage geneartor (V_{grid}), resistor (R_{grid}), and AC side inductor (L_{grid}) as a first order filter in series connection. The considered parameters of selected grid are listed in Table 5-13, and these values are taken from [48] for comparison purpose between eight switches MAC11-β_1 (1-DCS) vs eight switches PUC9 (1-DCS).

Table 5-13: Proposed Grid Model setup

Parameter	Value
RMS Grid voltage (V_{grid})	220 volts
Peak grid voltage	311 volts
Fundamental frequency (f_o)	50Hz
Phase Angle (θ)	0
Inductance (L_{grid})	2.5 mH
Resistance (R_{grid})	0.01 Ohm

5.2.2 Mathematical Modelling of MAC9, MAC7, and MAC11-β_1

MAC7 which is described in chapter 4; MAC7 has alpha and gamma modules, V_{main} is the single DC-source of this MAC, also it has two capacitors with voltages V_{sec0} for alpha's capacitor, V_{ab} is the output voltage of this inverter. The proposed MAC7 inverter generates 11 voltage levels (0, $\pm E$, $\pm 2E$, $\pm 3E$), where E= $\frac{V_{main}}{2}$ which is the voltage reference of each level, the nominal voltage for the V_{main} is equal to 2E, and $V_{C0 =}E$.

Also, MAC11-β_1 is the MAC inverter which is composed of alpha, beta1, and the gamma modules. It works in 1-DCS configuration, V_{main} is the single DC-source of this MAC, also it has two capacitors with voltages V_{sec0} for alpha's capacitor and V_{sec1} for beta's capacitor, V_{ab} is the output voltage of this inverter (for details in chapter 4).

The proposed MAC11-β_1 inverter generates 11 voltage levels (0, $\pm$E, $\pm$2E, $\pm$3E, $\pm$4E, $\pm$5E), where E= $\frac{V_{main}}{4}$ which is the voltage reference of each level, the nominal voltage for the V_{main} is equal to 4E, $V_{C0 =}$2E, and $V_{c1 =}$E.

The used control strategy and derivative equations is in [49]. The proposed general model has voltages of the single capacitor V_{c0} (t) as in MAC9 and MAC7, and two capacitors V_{C0} (t) and V_{C1} (t) in MAC11-β_1, there are to be within the nominal voltage, also the grid current should track grid current-reference, the generated output voltage of proposed inverter is based on voltage-reference value I and switching states of B/C/D sequence. For MAC11-β_1, Tables 5-5 which states that, there are twenty-two redundant states which are determined B/C/D sequence of charging and discharging behavior of the capacitors voltage to keep their levels the nominal value.

$$V_{inv} = S_{main}V_{main}+ S_0V_{C0} + S_1V_{C1} + \ldots + S_NV_{CN} \tag{5-1}$$

For N=0 MAC9 and MAC7

$$V_i = S_{main}V_{main}+ S_0V_{C0} \tag{5-2}$$

For N=1 MAC11-β1

$$V_i = S_{main}V_{main}+ S_0V_{C0 +}+ S_1V_{C1} \tag{5-3}$$

while the grid current dynamics based on the proposed Model can be expressed as:

$$\frac{dI_{grid}}{dt} = \frac{R_{grid}}{L_{grid}} i_{grid} + \frac{1}{L_{grid}} (v_{inv} - v_{grid}) \tag{5-4}$$

Tables 5-14, 5-15, and 5-16 illustrate the summarized switching states for single DC-source MAC9 (M-DCS), MAC7 (1-DCS), and MAC11-β_1 (1-DCS). For example, state 3 in Table 5-14 refers to ($V_{main} - V_{C0}$) voltage level value.

Table 5-14: Summarized switching states for MAC9

St.	S_{main}	S_0
1	1	1
2	1	0
3	1	-1
4	0	1
5	0	0
5R	0	0
6	0	1
7	1	-1
8	1	0
9	1	1

Table 5-15: Summarized switching states for MAC7

St.	S_{main}	S_0
1	1	1
2	1	0
3	1	-1
3R	0	1
4	0	0
4R	0	0
5	0	1
5R	1	-1
6	1	0
7	1	1

Table 5-16: Summarized switching states for MAC11-β_1

St.	S_{main}	S_0	S_1
1	1	1	-1
1R	1	0	1
2	1	0	0
3	1	0	-1
3R	1	-1	1
4	1	-1	0
4R	0	1	0

5	0	1	-1
5R	0	0	1
6	0	0	0
6R	0	0	0
7	0	0	-1
7R	0	-1	1
8	0	-1	0
8R	-1	1	0
9	-1	1	-1
9R	-1	0	1
10	-1	0	0
11	-1	0	-1
11R	-1	-1	1

KVL is applied on MAC11-β_1, relations between grid current $i_{grid}(t)$, capacitors voltages $V_{C(0)}(t)$, ..., $V_{C(N-1)}(t)$, and $V_{C(N)}(t)$, V_{main} level and the switching states S_m can be expressed as following equation:

$$C_N \frac{dV_{CN}}{dt} = - S_N I_{grid}(t) \tag{5-5}$$

For N=0 MAC9 and MAC7

$$C_0 \frac{dV_{C0}}{dt} = - S_0 I_{grid}(t) \tag{5-6}$$

For N=1

$$C_1 \frac{dV_{C1}}{dt} = - S_1 I_{grid}(t) \tag{5-7}$$

The changing of grid current is expressed as:

$$L_{grid} \frac{dI_{grid}}{dt} = S_{main} V_{main}(t) + S_0 V_{C0}(t) + S_1 V_{C1}(t) + ... + S_N V_{C(N)}(t) - R_{grid} I_{grid} -$$

$$V_{grid}(t) \tag{5-8}$$

For N=0 MAC7 and MAC9

$$L_{grid} \frac{dI_{grid}}{dt} = S_{main} V_{main}(t) + S_0 V_{C0}(t) - R_{grid} I_{grid} - V_{grid}(t) \tag{5-9}$$

For N=1 MAC11-β_1

$$L_{grid} \frac{dIgrid}{dt} = S_{main} V_{main}(t) + S_0 V_{C0}(t) + S_1 V_{C1}(t) - R_{grid} I_{grid} - V_{grid}(t)$$

(5-10)

Where:

V_{main}: DC-source

V_{C0}, V_{C1}, …, V_{CN}: voltages of capacitors

C_0: Capacitor of Alpha-module

C_1: Capacitor (1) of Beta cell number 1

C_N: Capacitor (N) of Beta cell number N

M_1, M_2, M_3, and M_4: Switching states for alpha and beta switches

H_1 and H_2: Switching states for gamma switches

L_{grid}: inductance of grid filter

R_{grid}: inductance of grid filter

$I_{grid}(t)$: Grid current

$V_{grid}(t)$: Grid voltage

5.2.3 Mathematical Modelling of FCS-MPC Technique

Control technique is used for two structures based on single DC-source MAC topology; MAC9, MAC7, and MAC11-β_1 to keep the voltages level of the two capacitors at their nominal voltages while the output current is tracking the grid current reference. On other hand, each controlled parameters (such as V_{C0} (t), V_{C1} (t), and I_{grid}(t)) affect to the others, and vice versa, the complexity of control system is reduced, as result of that, the major feature of this selected technique: the switching states are considered as limitations and constraints on the control input of the system, this impacts the modulation levels is'nt required [50] and [51]. Normalizing the state variables by calculating there the maximal variations. These variations of proposed parameters will be used in the cost function calculation. As mentioned before, this control strategy is presented in [49]. All following equation are applied on MAC-β_1, for MAC9 and MAC7: set V_{C1}=0.

MPC has three major steps:

1. Model of Prediction

2. Objective Function

3. Algorithm of Optimization

5.2.3.1 Model of Prediction

Prediction of capacitors level voltages ($V_{C0}{}^{k+1}$, $V_{C1}{}^{k+1}$, ... , $V_{CN}{}^{k+1}$) and the grid current ($I_{grid}{}^{k+1}$) and for each switching inverter state (output voltage level which is generated by the proposed MAC inverter) in discrete equations of the controller system state variables. this model is simplification in the following step, the state variables behavior is simplified to calculate as semi-linear on a small sampling time. For this reason, the approximation of the state variable that found in equations (5-11) – (5-15) will be for each sampling time Ts using equation:

$$x^{k+1} = x^k + \dot{x}(t).T_s \qquad (5\text{-}11)$$

(k+1) sample of time in terms of recent sample (k); So, the predictions of state variables

$$V_{CN}{}^{k+1} = V_{CN}{}^k + (S_N).T_s \ I_{grid}{}^k \qquad (5\text{-}12)$$

For MAC7, MAC9, and MAC11-β1 capacitors voltage:

$$V_{C0}{}^{k+1} = V_{C0}{}^k + (S_0).\frac{T_s}{C0} \ I_{grid}{}^k \qquad (5\text{-}13)$$

$$V_{C1}{}^{k+1} = V_{C1}{}^k + (S_1).T_s \ I_{grid}{}^k \qquad (5\text{-}14)$$

(k+1) sample of time

$$I_{grid}{}^{k+1} = I_{grid}{}^k + S_{main}.V_{main}{}^k + S_0.V_{C0}{}^k + S_1.V_{C1}{}^k + ... + S_1.V_{CN}{}^k - V^k{}_{grid} \qquad (5\text{-}15)$$

Also [49] control presents final derivative equations that are expressed the variation of inverter voltage with respect the change of grid current:

$$V_{inv} = V_{grid} + R_{grid}.I_{grid} + L_{grid}.\frac{dI_{grid}}{dt} \qquad (5\text{-}16)$$

And then

$$I_{grid}^{k+1} = (1 - \frac{R_{grid}.T_s}{L_{grid}}) I_{grid}^{k} + \frac{T_s}{L_{grid}} .(V_{inv}^{k} - V_{grid}) \qquad (5\text{-}17)$$

State Variables Normalization

The variation ranges of the proposed parameters (voltages & current) aren't matter in MPC technique whose aim to reduce the error between the voltage and current references and measured values, this refers to select the switching state that gives the minimal error, equation (5-12).

5.2.3.2 Calculation of Cost Function

Cost function (g_C) which is the objective function of the proposed control strategy, g_C is aimed to minimize the error which is difference between the predicted state variables voltages (V_{C0}^{k+1}, V_{C1}^{k+1}, ... ,V_{CN}^{k+1} and I_{grid}^{k+1}) and their references values. The cost function can be found as the following equation [49]:

$$g_c = K_g./I_{grid}*\text{-}I_{grid}(k+1)/ + K_{C0}./V_{C0}*\text{-}V_{C0}(k+1)/ + K_{C1}./V_{C1}*\text{-}V_{C1}(k+1)/ + ... + K_{CN}./V_{CN}* - V_{CN}(k+1)/ \qquad (5\text{-}18)$$

Where gc is the cost function

$V_{C0}*$ is the nominal voltage of the first capacitor C_0,

$V_{C1}*$ is the nominal voltage of the second capacitor C_1,

$V_{CN}*$ is the nominal voltage of the N capacitor C_N,

$i_{grid}*$ is the reference current and

K_g, K_{C0}, ..., and K_{CN} is the weighting factor that can be adjusted to find aimed results of this MAC control model.

5.2.3.3 Algorithm of Control Optimization

In this section, the proposed algorithm of MPC is described to achieve the optimal state for each sample, this algorithm has a critical factor which is Weighting factor, this factor effect appears on two main parameters: the ripple of capacitors voltage level and THD values, it based on estimating parameters called weighting factors.

- **Weighting Factors (K_w)**

Weighting factor is a tuning mathematical factor; this estimated factor has sensitive role in cost calculations in the proposed inverter control stability and performance [52]. The tuning of the weighting factor of grid current and capacitors voltage: K_g, K_{C0}, …, and K_{CN} is required to select for reducing the THD value of the grid current signal and the improve the voltage ripple of the capacitors (V_{C0}, $V_{C1, ...,}$ and V_{CN}). %. K_g, K_{C0}, …, and K_{CN} values selection based on the performance indicators: THD of the grid current (I_{grid}), V_{C0}, $V_{C1, ..., and}$ V_{CN} voltages ripple.

Figure 5-13 illustrate the proposed control method for MAC inverter in 1-DC configuration.
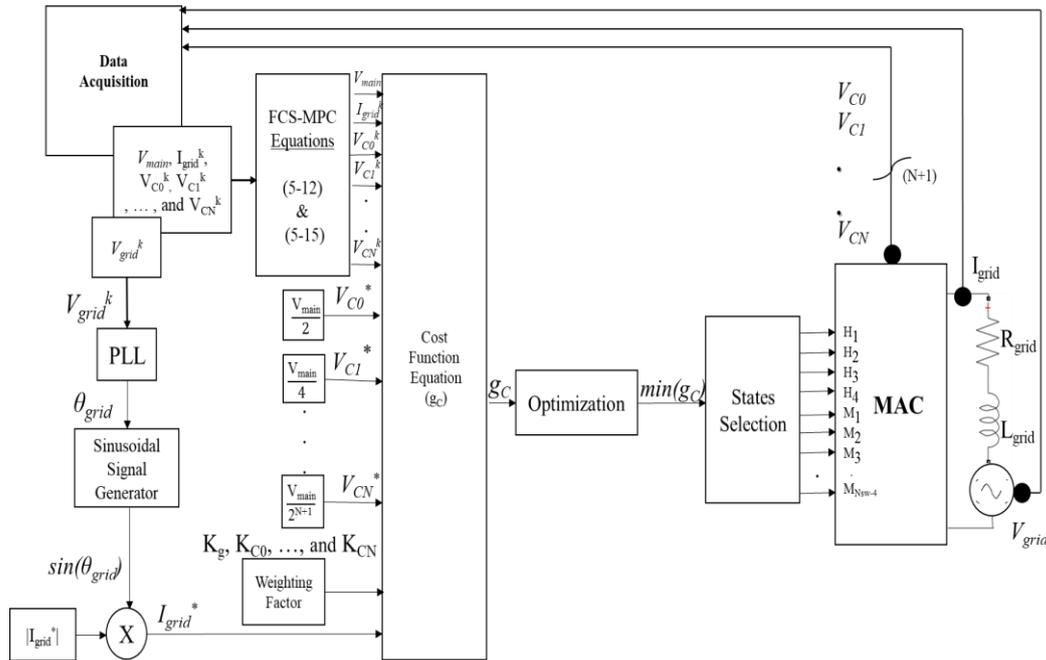
Figure 5-13: The proposed control method for grid-connected MAC inverter

The process of the proposed control strategy is illustrated by a flow chart in Figure 5-14, in start; acquisition the data values for variable parameters as samples (such as V_{C0} (t), V_{C1} (t), …, V_{CN} (t), and I_{grid}(t), …, etc.), then initializing the start and reference values (V_{C0}, V_{C1}, …, V_{CN}, I_{grid}, …), equations (5-1) & (5-17) are applied to find instantaneous of grid current, next step is finding the value of cost function value for this sample, the optimal value is the minimum. Finally, applying the suitable switching state based on minimum g_C value, and then waiting new sample read.
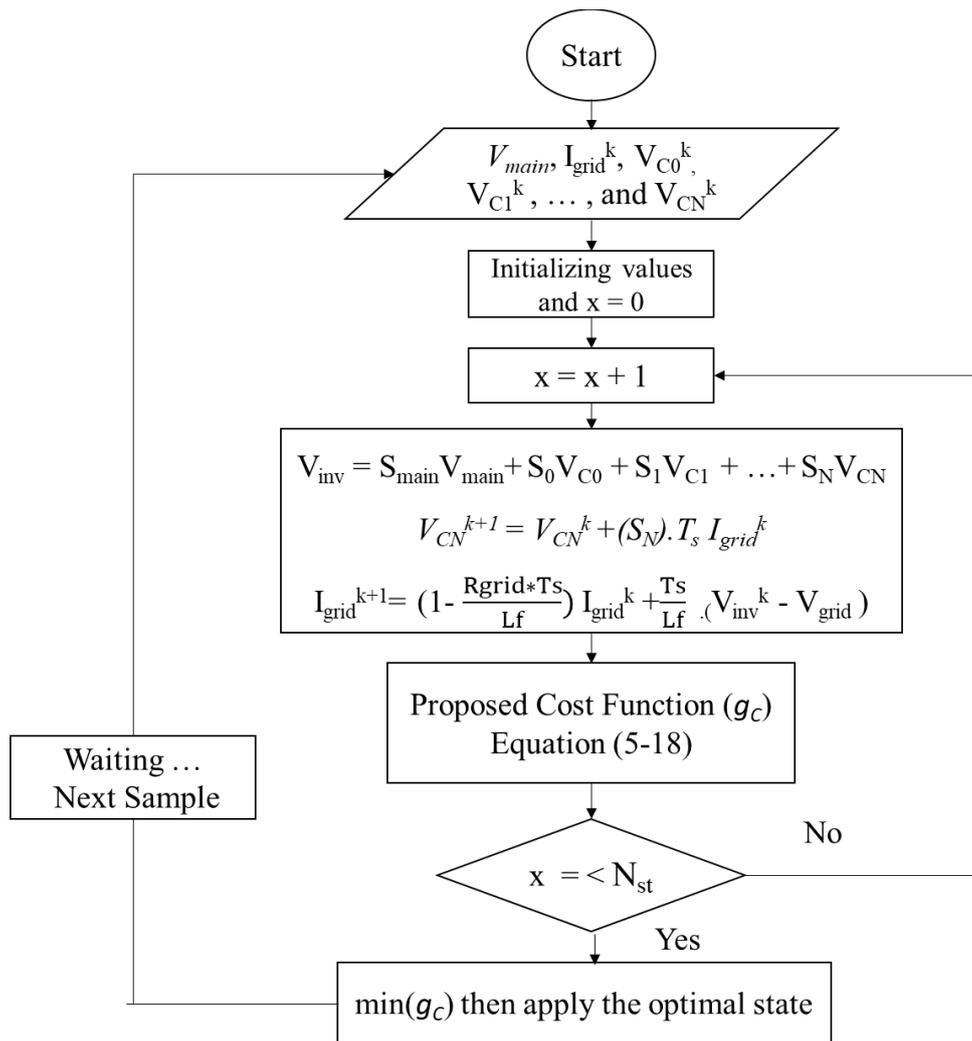
Figure 5-14: Flow chart of MPC for grid-connected MAC inverter

Simulation results of the designed MAC forms validation are shown in the next chapter which also represents the comparison parameters of these structures such as THD values for the voltage and current waveforms of each form. Also, step changing scenarios on MAC11-β_1 (1-DCS) in Grid-connected case.

CHAPTER 6
SIMULATION RESULTS

This chapter presents the validation of the proposed MAC topology forms using SIMULINK/MATLAB, this work is divided to two major parts based on used source operation configuration; first one: Several multiple DC-sources MAC forms are controlled using open-loop SPWM technique in Standalone in M-DCS, and the second: single DC-source MAC9(M-DCS), MAC7(1-DCS), and MAC11-β_1(1-DCS) are controlled using MPC method in Grid-Connected.

6.1 Open-Loop Standalone

This simulation is to verify proposed multiple DC-sources MAC (M-DCS) in the following forms:

- Basic-MAC (M-DCS): MAC9.

- Extended-MAC: MAC21-β_1, MAC45-2β_1, MAC23-$\beta2$, MAC53-2β_2, MAC27-β_3 positive half-cycle of MAC81-2β_3, and MAC49-2α_c, these structures are controlled using open-loop SPWM technique based on bipolar control in Standalone with DPF near unity (DPF=0.99) for validation purpose. This section presents different forms of MAC without using a filter. Also, the proposed MAC-β_1 which based on 1-DCS ratio configuration is presented for single Beta-1 with 13 levels, but it's simulated with multiple DC-sources. Figure 6-1 shows the load Model.
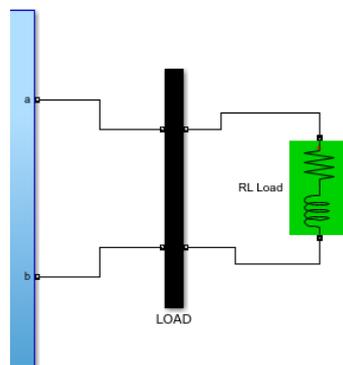
Figure 6-1: Load Model connected to output nodes (a and b) of MAC

The parameters of: general MAC and load Matlab Model inverter and the load setup are illustrated in Table 6-1. Displacement Power Factor (DPF) is equal to cos (θ) and assumed to 0.999 near unity for minimum voltage spikes catching purpose.

Table 6-1: General MAC and Load Matlab Model Parameters

Parameter	Symbol, Unit	Value
MAC Settings		
Output AC voltage (peak)	V_{inv}, V	311
Output AC voltage (RMS)	V_{RMS}, Vrms	220
Switching Frequency	f_{SW}, Hz	2050
Sampling Time	Ts, µs	25
Fundamental frequency	f_O, Hz	50
Inductive Load for *5 KVA*		
Displacement Power Factor	DPF	0.999
Real Power Load	P_L, KW	4.995
Reactive Power Load	Q_L, KVAr	0.2

6.1.1 Multiple DC-sources MAC9(M-DCS)

Figure 6-2 shows the Simulink model of MAC9 in Standalone case. In this case the inverter is feeding an inductive load.
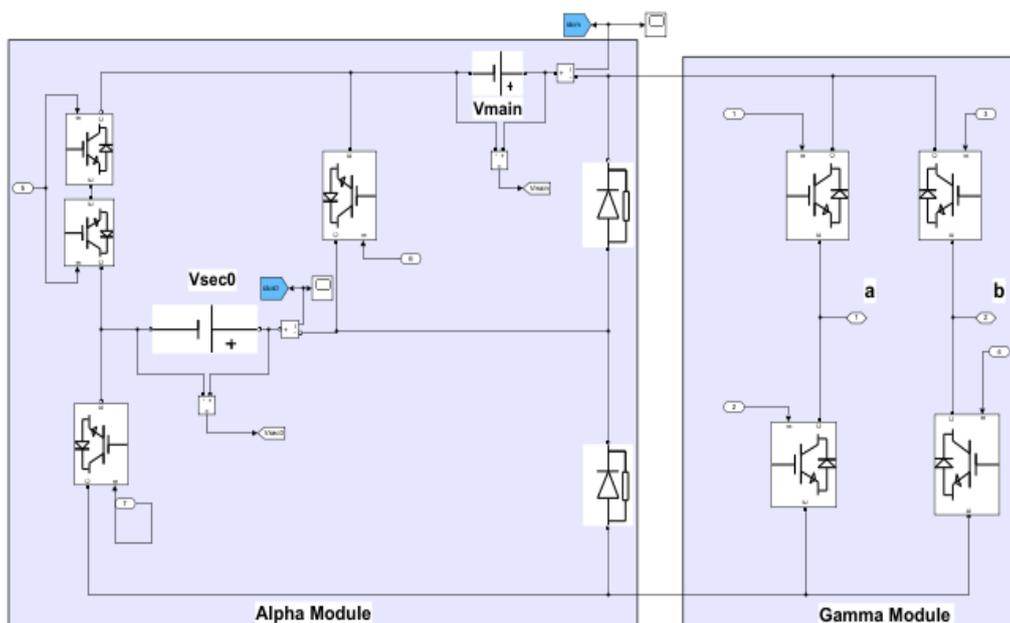
Figure 6-2: MAC9 MATLAB model using DC-sources

The parameters of MAC9 inverter setup are illustrated in Table 6-2.

Table 6-2: Specifications of Proposed MAC9 model

Parameter	Symbol, Unit	Value
MAC9		
Alpha Main DC voltage	V_{main}, V	3E=300
Alpha Secondary DC voltage	V_{sec0}, V	E=100
Number of Levels	N_{level}	9

The LS-SPWM eight-carriers (V_{cr}) and control signals (V_{cn}) are illustrated in Figure 6-3.
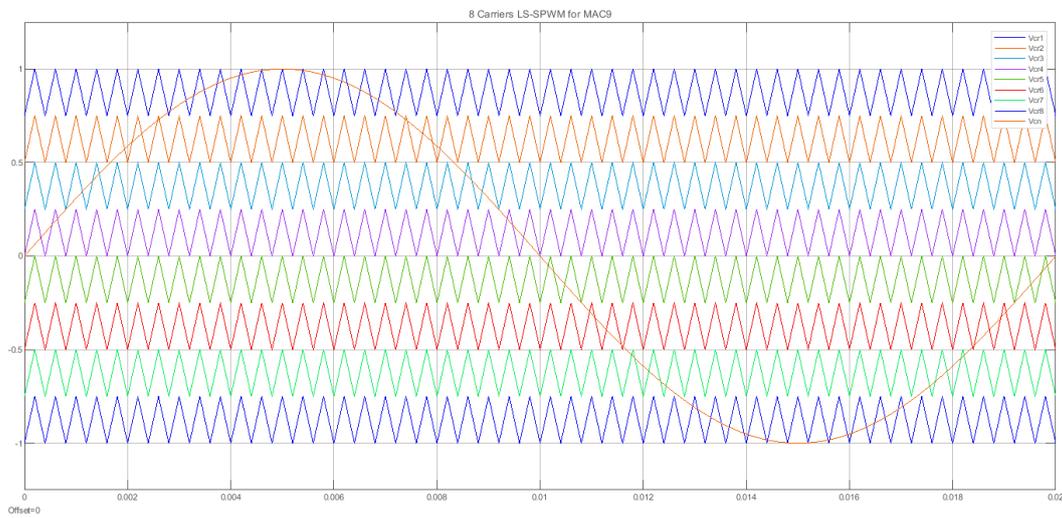
Figure 6-3: LS-SPWM eight-carrier and control signal

Output voltage (V_{inv}) with clear nine-level voltage and semi-sine load current waveform (I_L) are shown in Figure 6-4.
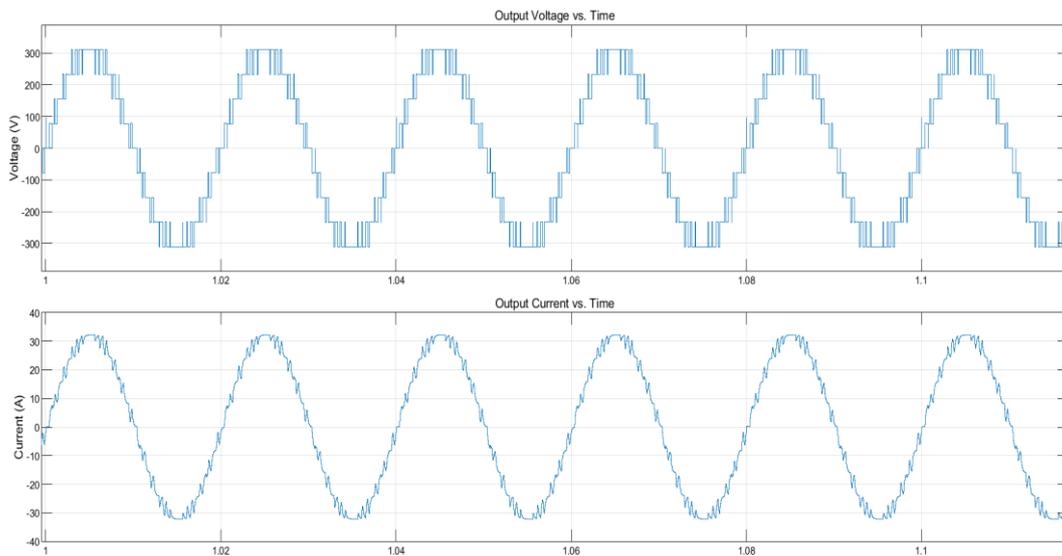
Figure 6-4: 9L-V$_{inv}$, and I$_L$ waveforms

After analyzing the output voltage and current waveforms of MAC9. THD of output voltage (THDv) is 13.72%, and THD of output current (THDi) is 5.91%, as shown in Figure 6-5.
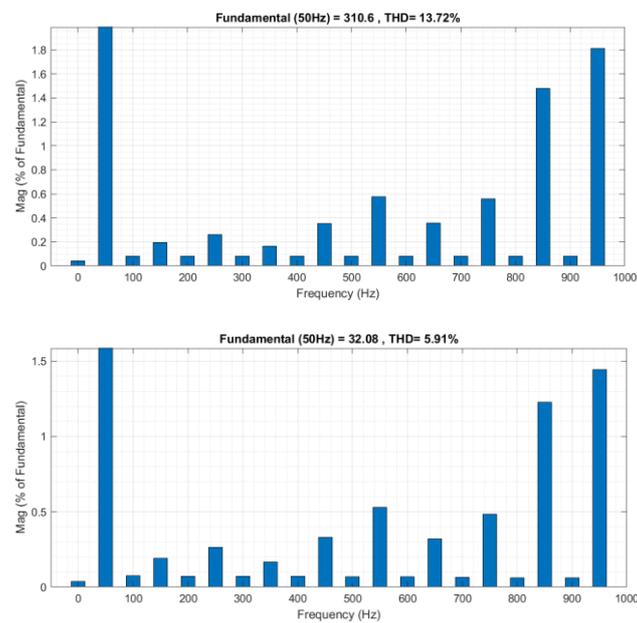
Figure 6-5: Simulink FFT Analysis of Vinv and IL , THD (%) for MAC9

6.1.2 MAC- β_1 (M-DCS)

This structure has two choices of desired Level count based on asymmetrical source ratio; the proposed M-DCS configurations, MAC13-β_1 and MAC21-β_1, and MAC45-2β_1.

6.1.2.1 MAC13-β_1

Figure 6-6 shows the Simulink model of MAC13-β_1 in Standalone case and based on 1-DCS configuration. In this case the inverter is feeding an inductive load, this scheme is presented in 1-DCS configuration.
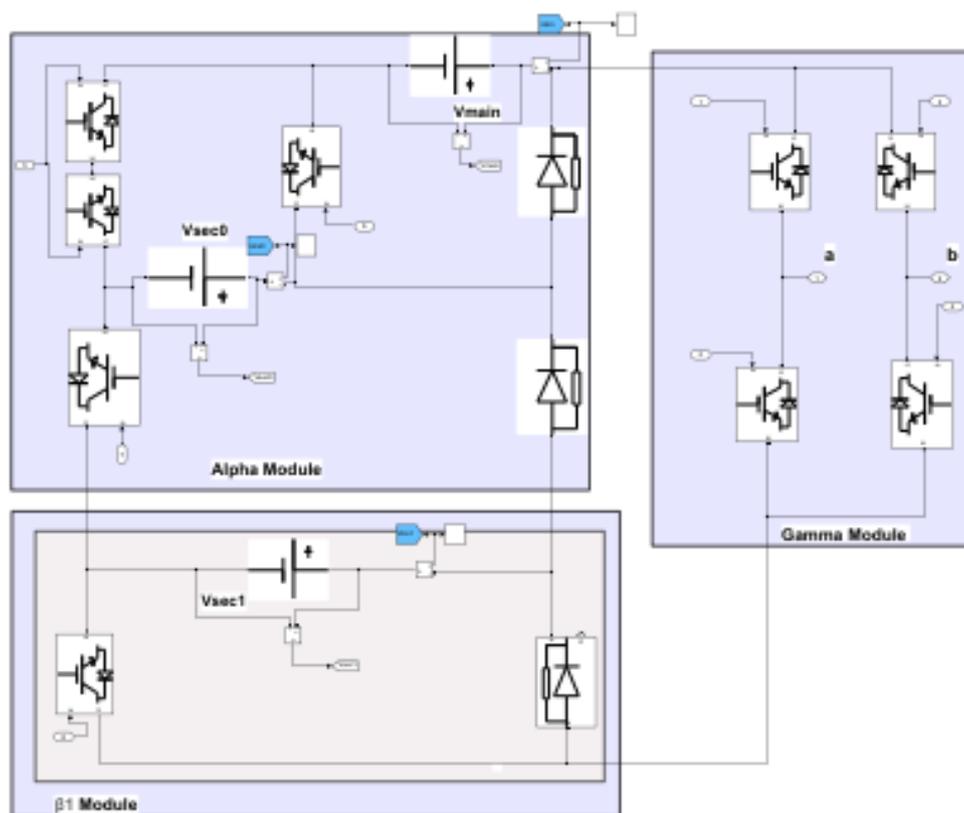
Figure 6-6: MAC-β1 MATLAB model using DC-sources for MAC13-β₁ & MAC21-β₁

forms

The parameters of MAC13-β_1 inverter setup are illustrated, Table 6-3.

Table 6-3: Specifications of Proposed MAC13-β_1 Model

Parameter	Symbol, Unit	Value
MAC13-β1		
Alpha Main DC voltage (V$_{main}$)	V$_{main}$, V	4E
Alpha Secondary DC voltage	V$_{sec0}$, V	2E
Beta-1 DC voltage	V$_{sec1}$, V	E=$\frac{311}{6}$
Number of Levels	N$_{level}$	13

The LS-SPWM twelve-carriers (V$_{cr}$) and control signals (V$_{cn}$) are illustrated in Figure 6-7.
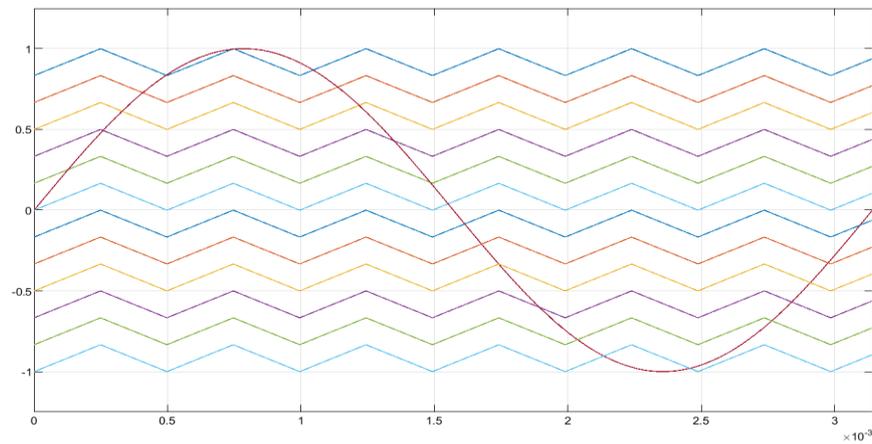
Figure 6-7: LS-SPWM twelve-carriers and control signal

Output voltage (V$_{inv}$) with clear 13-level voltage and semi-sine load current waveform (I$_L$) are shown in Figure 6-8.
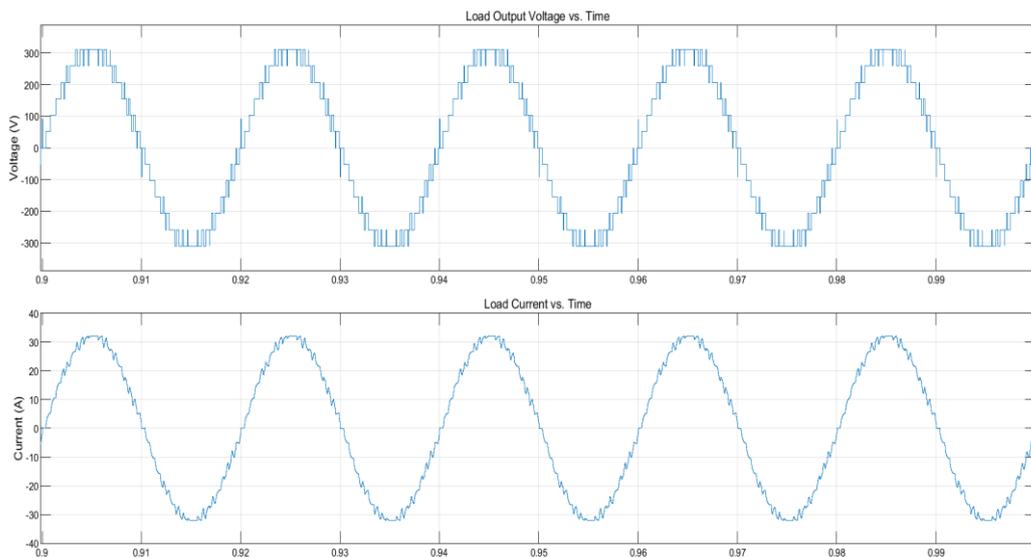
Figure 6-8: 13L-V_{inv}, and I_L waveforms

After analyzing the output voltage and current waveforms of MAC13-β_1. THD of output voltage (THDv) is 9.52%, and THD of output current (THDi) is 4.08%, as shown in Figure 6-9.
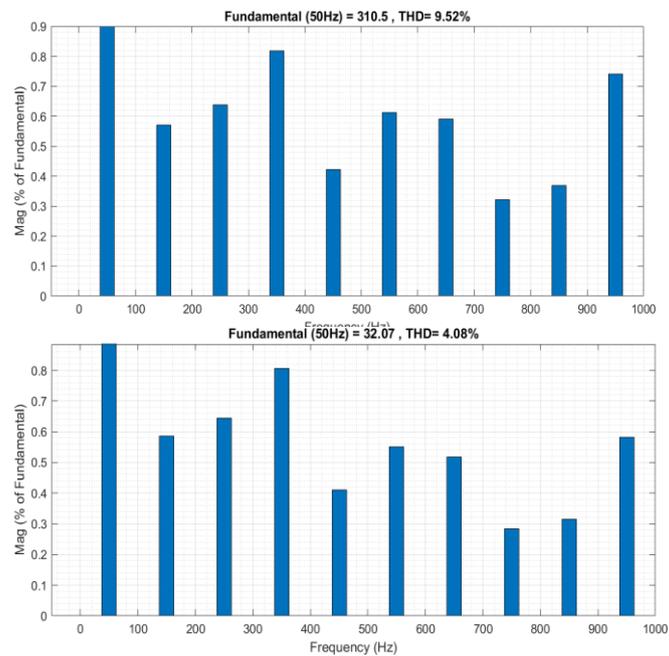
Figure 6-9: Simulink FFT Analysis of V_{inv} and I_L, THD (%) for MAC13-β_1

6.1.2.2 MAC21-β_1

Figure 6-6 shows the Simulink model of MAC21-β_1 in Standalone case and based on 1-DCS configuration. In this case the inverter is feeding an inductive load, this form has the same scheme of MAC21-β_1. The parameters of MAC21-β_1 inverter setup are illustrated in Table 6-4.

Table 6-4: Specifications of Proposed MAC21-β₁ Model

Parameter	Symbol, Unit	Value
MAC21-β1		
Alpha Main DC voltage (V_main)	V_{main}, V	7E
Alpha Secondary DC voltage	V_{sec0}, V	3E
Beta-1 DC voltage	V_{sec1}, V	$E=\frac{311}{10}$
Number of Levels	N_{level}	21

The LS-SPWM twelve-carriers (V_{cr}) and control signals (V_{cn}) are illustrated in Figure 6-10.
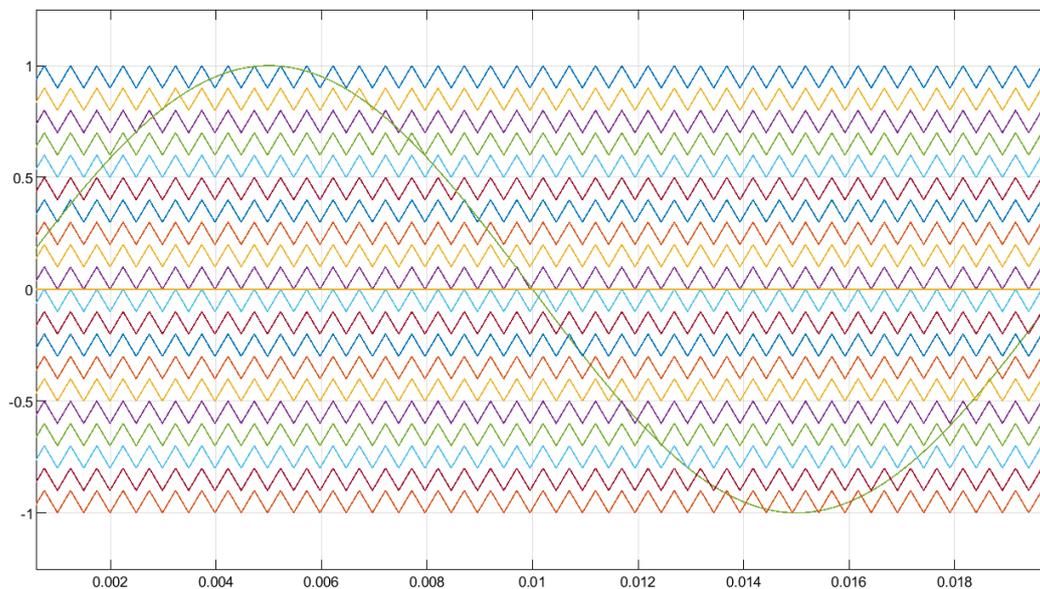
Figure 6-10: LS-SPWM 20-carriers and control signal

Output voltage (V_{inv}) with clear 21-level voltage and semi-sine load current waveform (I_L) are shown in Figure 6-11.
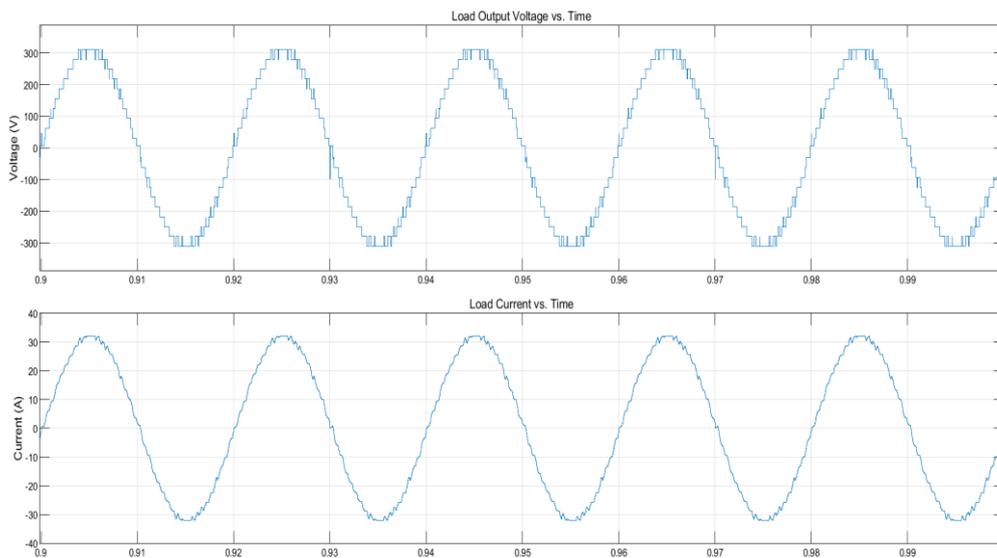
Figure 6-11: 21L-V_{inv}, and I_L waveforms

After analyzing the output voltage and current waveforms of MAC21-β_1. THD of output voltage (THDv) is 5.54%, and THD of output current (THDi) is 2.65%, as shown in Figure 6-12.
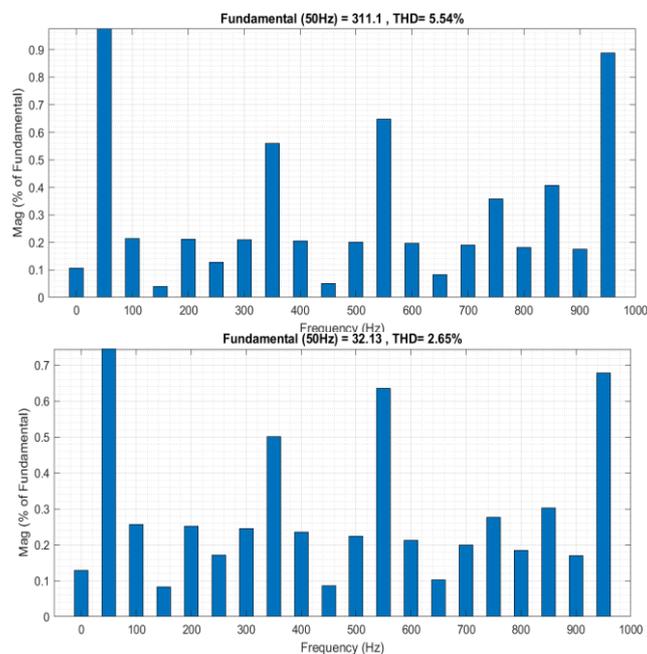
Figure 6-12: Simulink FFT Analysis of V_{inv} and I_L, THD (%) for MAC21-β_1

6.1.2.3 MAC45-2β₁

Figure 6-13 shows the Simulink model of MAC45-2β₁ in Standalone case and based on 1-DCS configuration. In this case the inverter is feeding an inductive load, this form has the same scheme of MAC45-2β₁, but it's designed for M-DCS.
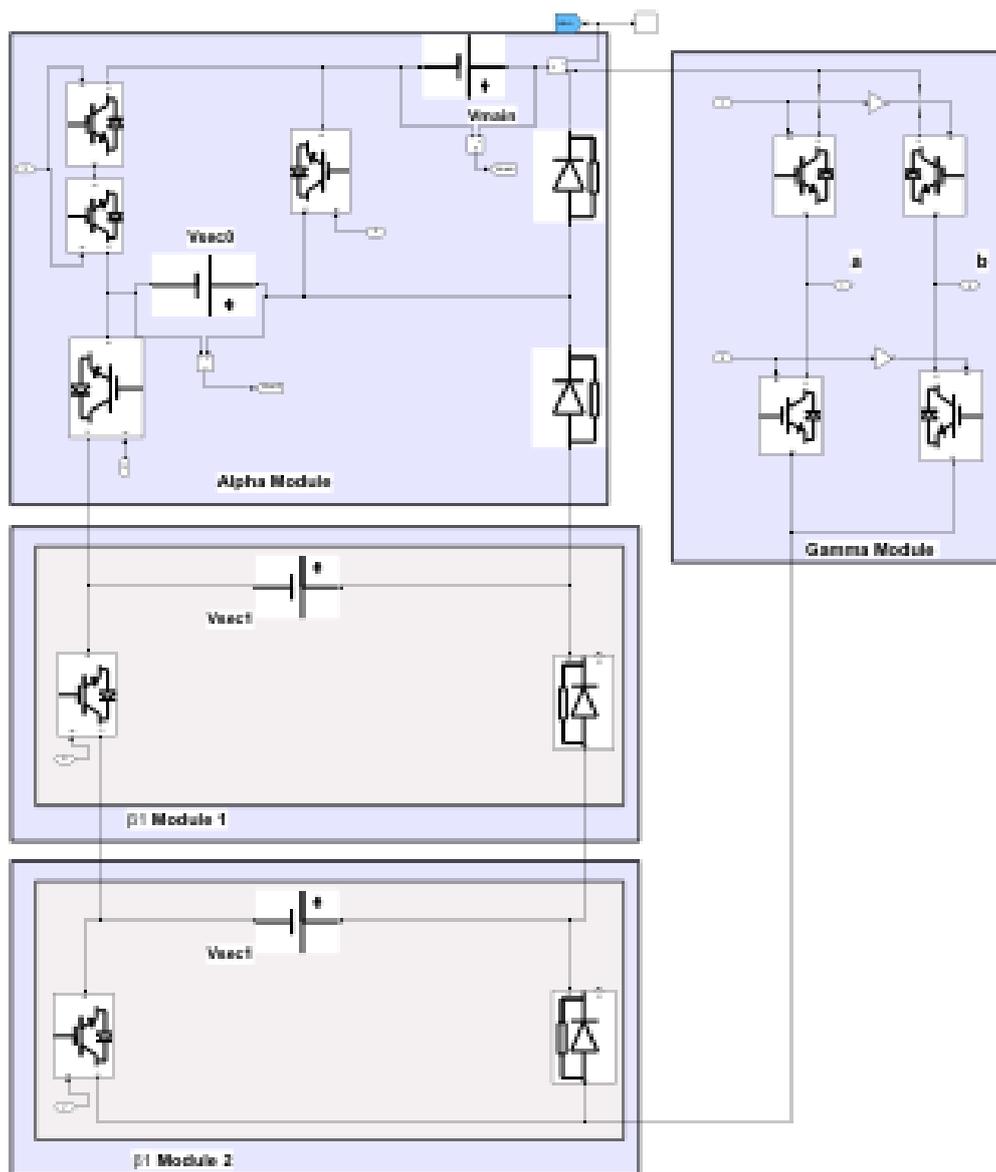
Figure 6-13: MAC45-2β₁ MATLAB Model using DC-sources

The parameters of MAC45-2β_1 inverter setup are illustrated in Table 6-5.

Table 6-5: Specifications of Proposed MAC45-2β_1 Model

Parameter	Symbol, Unit	Value
MAC45-2β_1		
Alpha Main DC voltage (V_{main})	V_{main}, V	15E
Alpha Secondary DC voltage	V_{sec0}, V	7E
First Beta-1 DC voltage	V_{sec1}, V	3E
Second Beta-1 DC voltage	V_{sec2}, V	$E=\frac{311}{22}$
Number of Levels	N_{level}	45

The LS-SPWM twelve-carriers (V_{cr}) and control signals (V_{cn}) are illustrated in Figure 6-14.
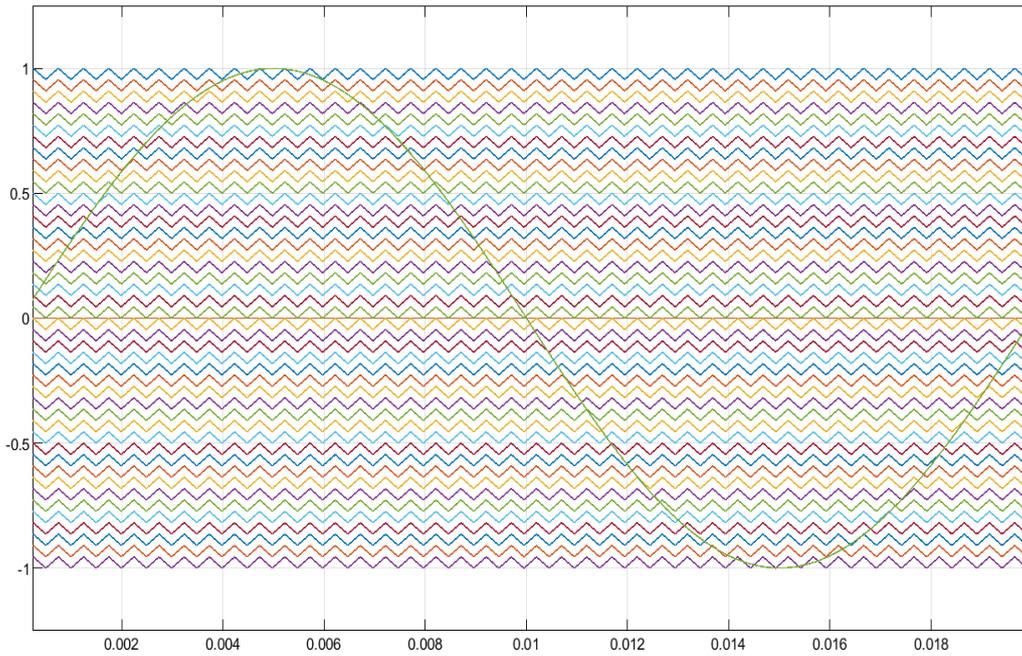
Figure 6-14: LS-SPWM 44-carriers and control signal

Output voltage (V_{inv}) with clear 44-level voltage and semi-sine load current waveform (I_L) are shown in Figure 6-15.
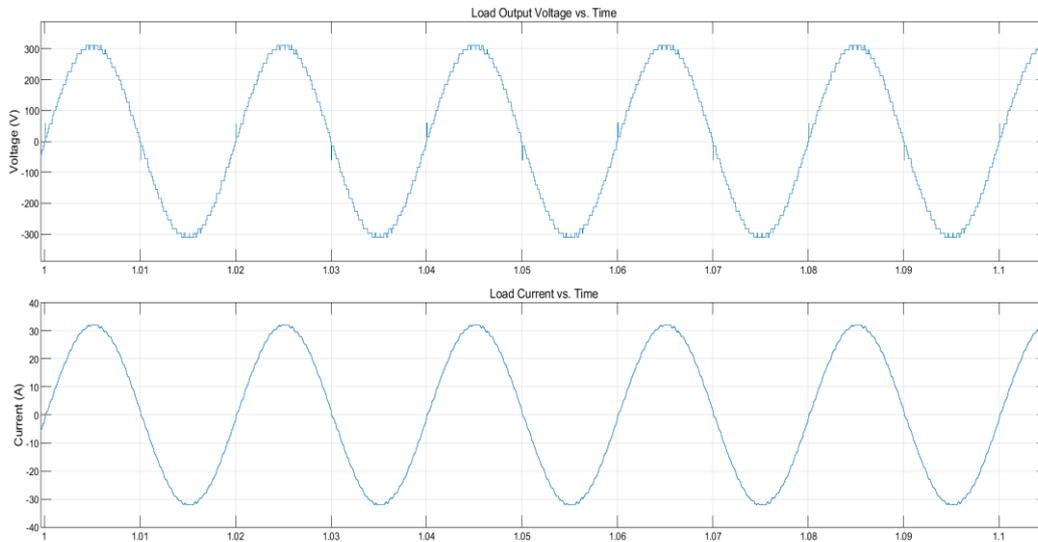
Figure 6-15: 45L-V_{inv}, and I_L waveforms

After analyzing the output voltage and current waveforms of MAC45-2β_1. THD of output voltage (THDv) is 2.88%, and THD of output current (THDi) is 1.2%, as shown in Figure 6-16.
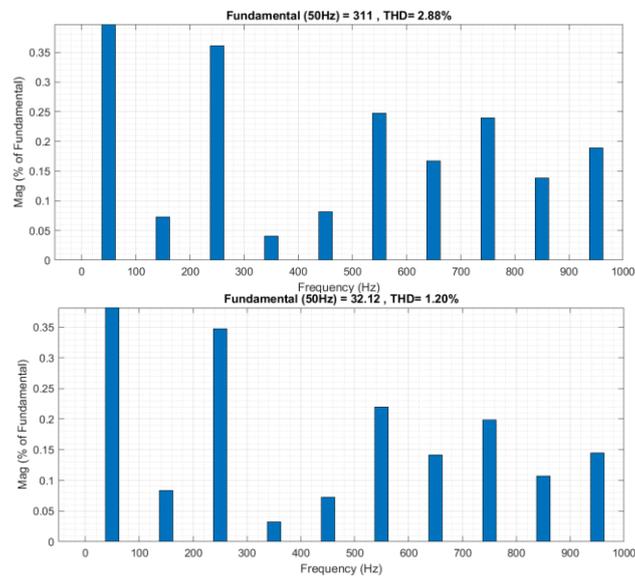
Figure 6-16: Simulink FFT Analysis of V_{inv} and I_L, THD (%) for MAC45-2β_1

6.1.3 MAC-β_2 (M-DCS)

This structure has single choice of desired Level count based on asymmetrical source ratio; the proposed M-DCS configuration, MAC23-β_2, and MAC53-2β_2.

6.1.3.1 MAC23-β_2

Figure 6-17 shows the Simulink model of MAC23-β_2 in Standalone case. In this case the inverter is feeding an inductive load, this form has the same scheme of MAC23-β_2.
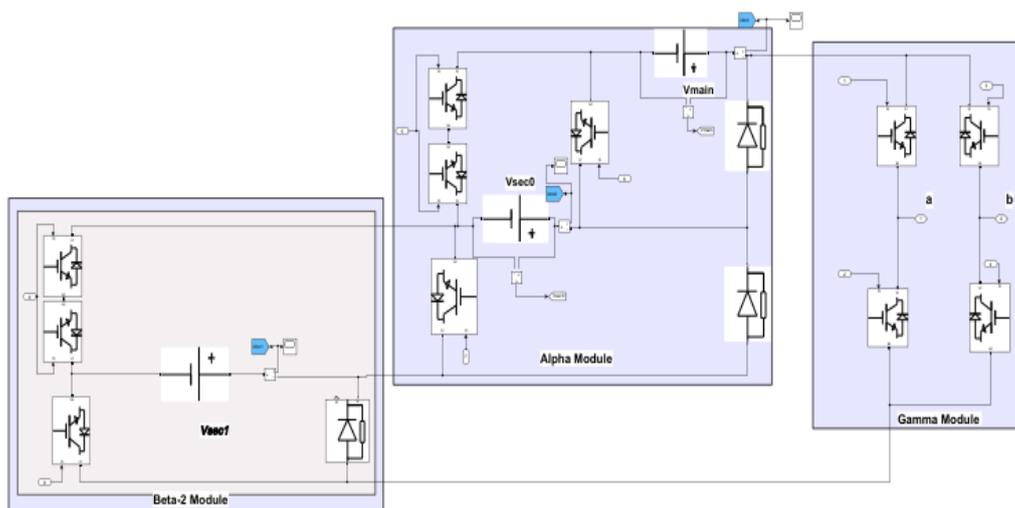
Figure 6-17: MAC23-β_2 MATLAB Model using DC-sources

The parameters of MAC23- β_2 inverter setup are illustrated in Table 6-6.

Table 6-6: Specifications of proposed MAC23-β_2 model

Parameter	Symbol, Unit	Value
MAC23-β_2		
Alpha Main DC voltage (V$_{main}$)	V_{main}, V	7E
Alpha Secondary DC voltage	V_{sec0}, V	3E
Beta-2 DC voltage	V_{sec1}, V	$E=\frac{311}{11}$
Number of Levels	N_{level}	23

The LS-SPWM twelve-carriers (V_{cr}) and control signals (V_{cn}) are illustrated in Figure 6-8.
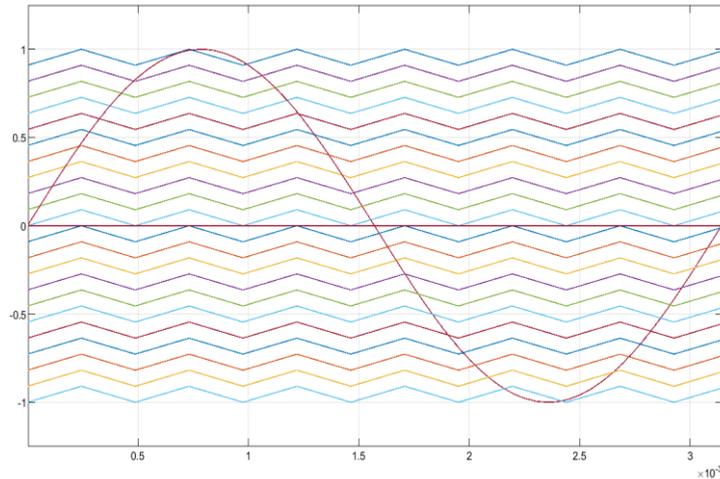
Figure 6-18: LS-SPWM 22-carriers and control signal

Output voltage (V_{inv}) with clear 23-level voltage and semi-sine load current waveform (I_L) are shown in Figure 6-19.
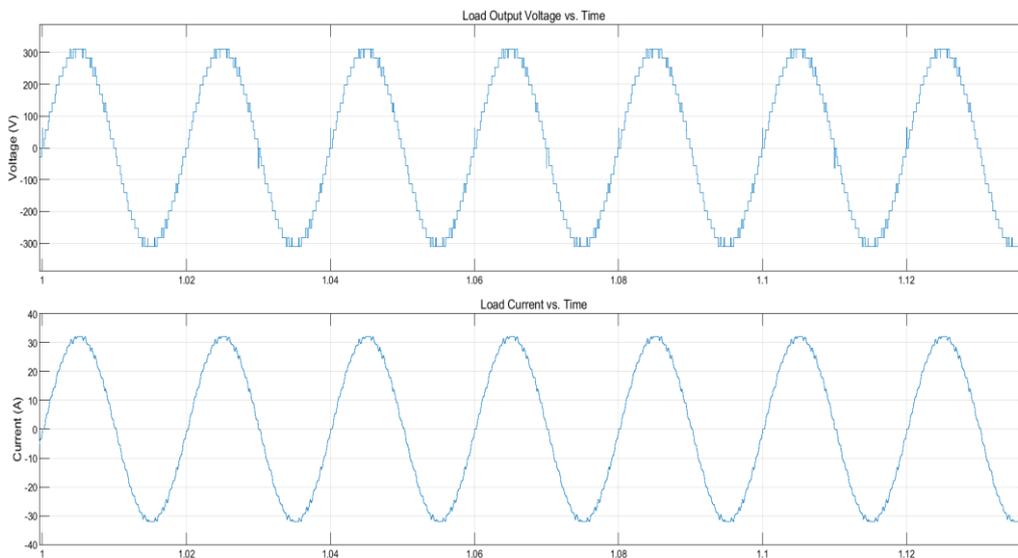
Figure 6-19: 23L-V_{inv}, and I_L waveforms

After analyzing the output voltage and current waveforms of MAC23-β_2. THD of output voltage (THDv) is 5.13%, and THD of output current (THDi) is 2.36%, as shown in Figure 6-20.
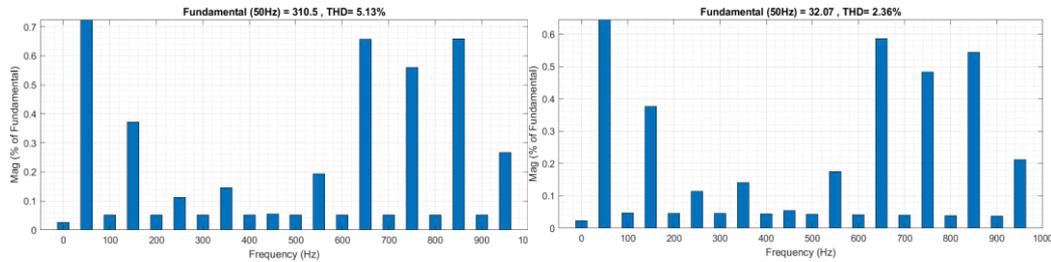
Figure 6-20: Simulink FFT Analysis of V_{inv} and I_L, THD (%) for MAC27-β_2

6.1.3.2 MAC53-2β_2

Figure 6-21 shows the Simulink model of MAC23-β_2 in Standalone case. In this case the inverter is feeding an inductive load, this form has the same scheme of MAC23-β_2.
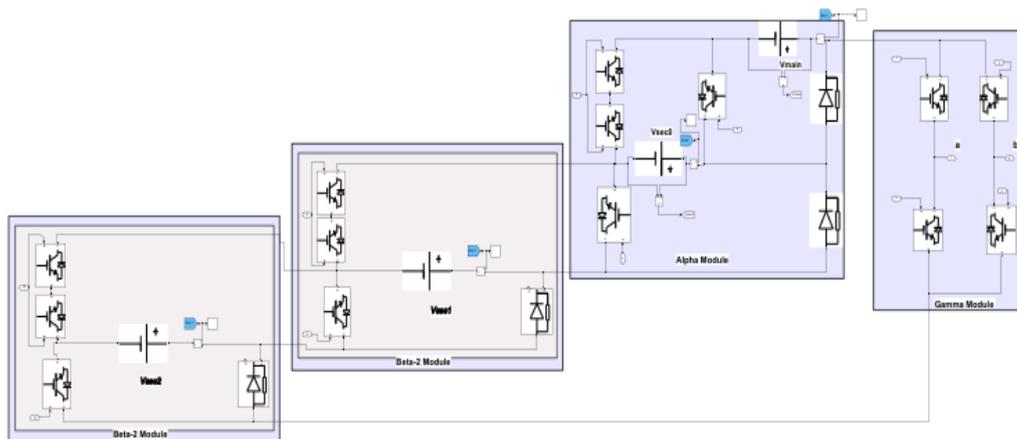
Figure 6-21: MAC53-2β_2 MATLAB Model using DC-sources

The parameters of MAC53-2β_2 inverter setup are illustrated in Table 6-7.

Table 6-7: Specifications of Proposed MAC53-β_2 Model with a load

Parameter	Symbol, Unit	Value
MAC53-2β_2		
Alpha Main DC voltage (V$_{main}$)	V$_{main}$, V	15E
Alpha Secondary DC voltage	V$_{sec0}$, V	7E
First Beta-2 DC voltage	V$_{sec1}$, V	3E
Second Beta-2 DC voltage	V$_{sec2}$, V	E=$\frac{311}{26}$
Number of Levels	N$_{level}$	53

The LS-SPWM twelve-carriers (V$_{cr}$) and control signals (V$_{cn}$) are illustrated in Figure 6-22.
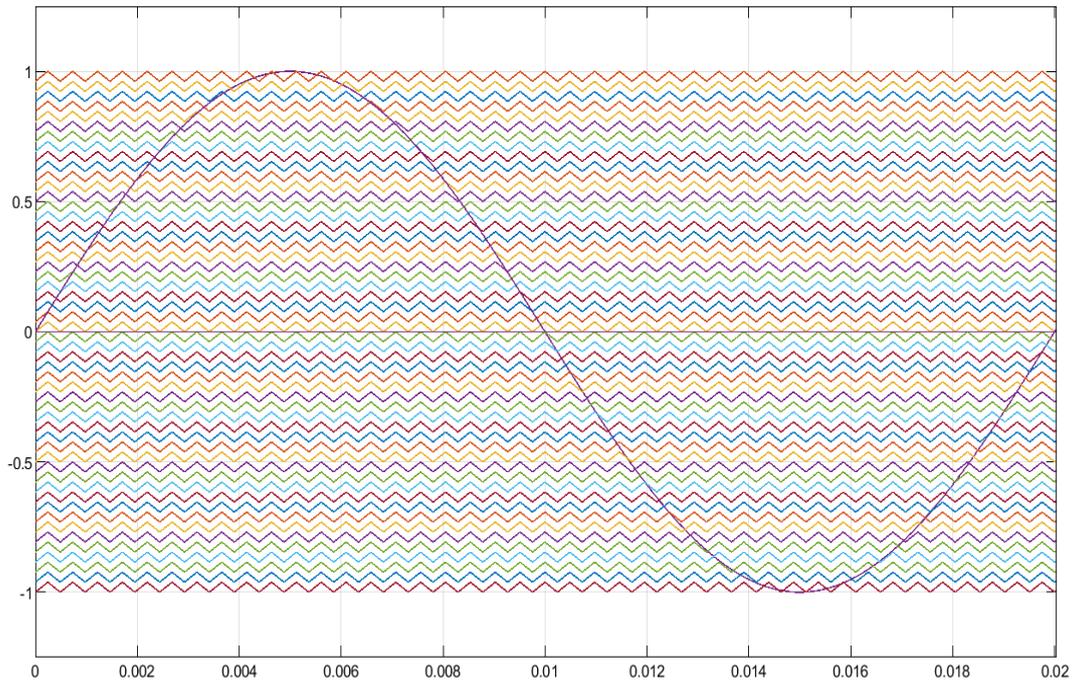
Figure 6-22: LS-SPWM 52-carriers and control signal

Output voltage (V$_{inv}$) with clear 53-level voltage and semi-sine load current waveform (I$_L$) are shown in Figure 6-23.
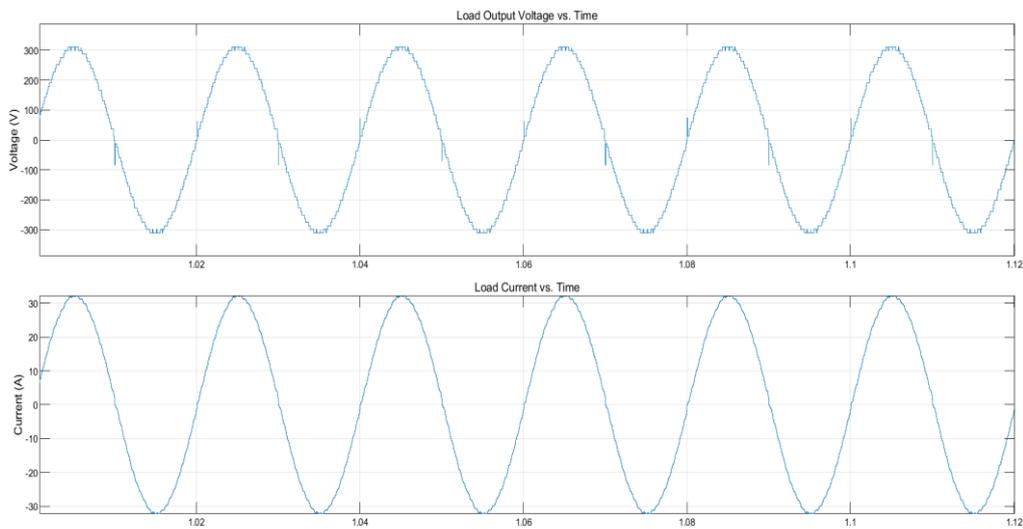
Figure 6-23: 53L-V$_{inv}$, and I$_L$ waveforms

After analyzing the output voltage and current waveforms of MAC53-2β_2. THD of output voltage (THDv) is 2.89%, and THD of output current (THDi) is 1.14%, as shown in Figure 6-24.
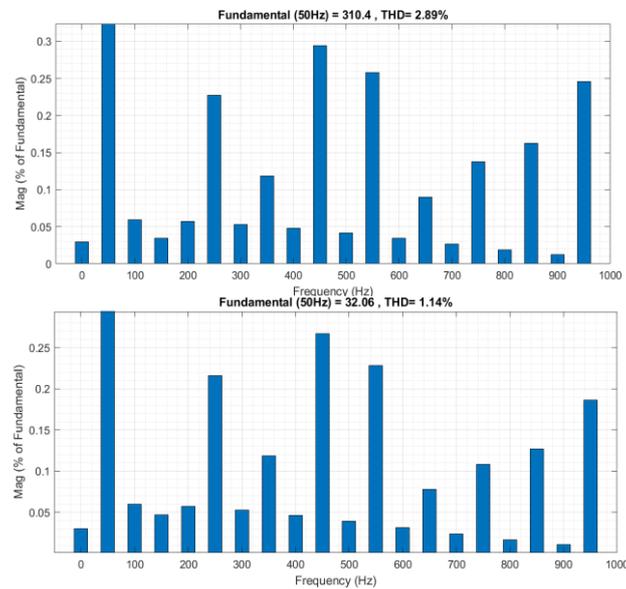
Figure 6-24: Simulink FFT Analysis of V$_{inv}$ and I$_L$, THD (%) for MAC53-2β_2

6.1.4 MAC- β₃ (M-DCS)

This structure has three choices of desired Level count based on asymmetrical source ratio; the proposed M-DCS configurations, MAC27-β₃, and MAC81-2β₃.

6.1.4.1 MAC27-β₃

Figure 6-25 shows the Simulink model of MAC27-β₃ in Standalone case. In this case the inverter is feeding an inductive load, this form has the same scheme of MAC27-β₃.
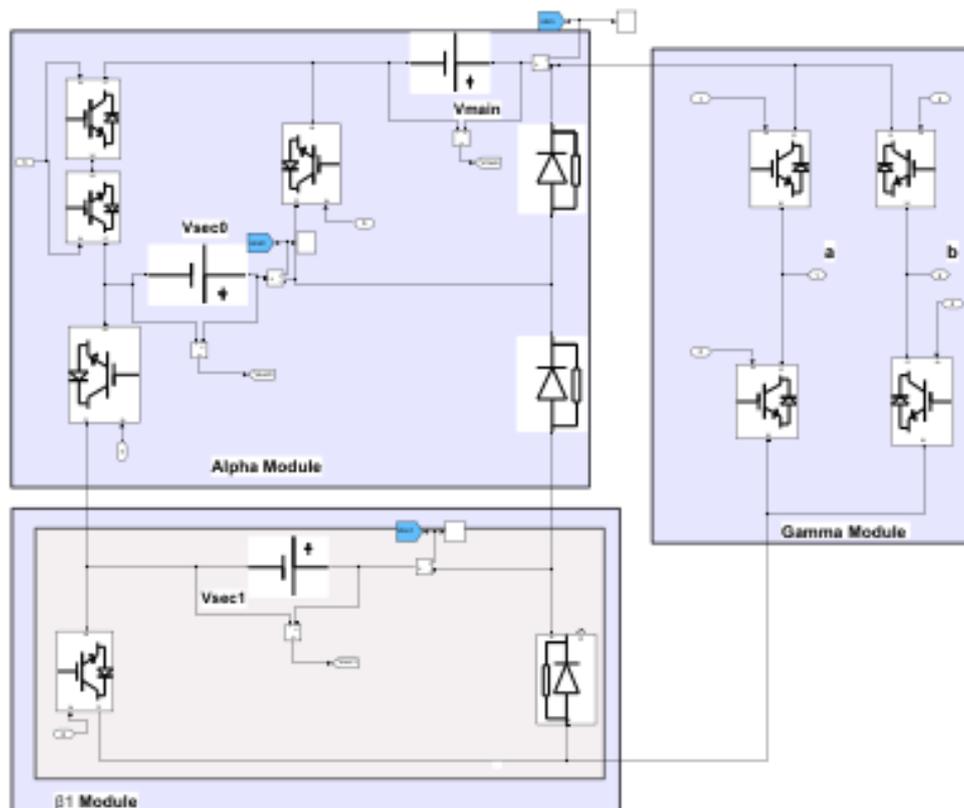
Figure 6-25: MAC27-β₃ MATLAB Model using DC-sources

The parameters of MAC27-β_3 inverter setup are illustrated in Table 6-8.

Table 6-8: Specifications of Proposed MAC27-β_3 Model with a load

Parameter	Symbol, Unit	Value
MAC27-β_3		
Alpha Main DC voltage (V_{main})	V_{main}, V	9E
Alpha Secondary DC voltage	V_{sec0}, V	3E
Beta-2 DC voltage	V_{sec1}, V	$E=\frac{311}{13}$
Number of Levels	N_{level}	27

The LS-SPWM 26-carriers (V_{cr}) and control signals (V_{cn}) are illustrated in Figure 6-26.
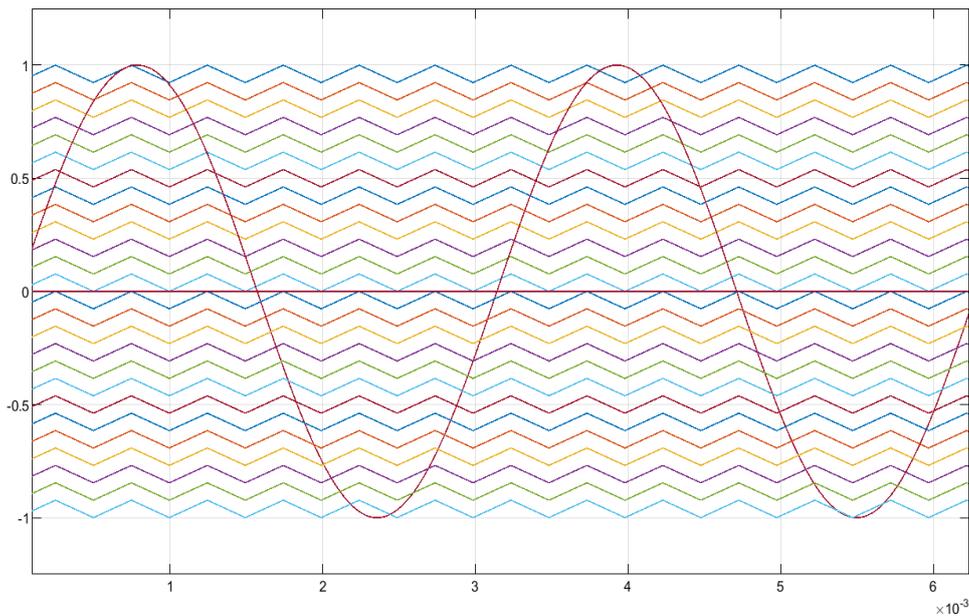
Figure 6-26: LS-SPWM 26-carriers and control signal

Output voltage (V_{inv}) with clear 27-level voltage and semi-sine load current waveform (I_L) are shown in Figure 6-27.
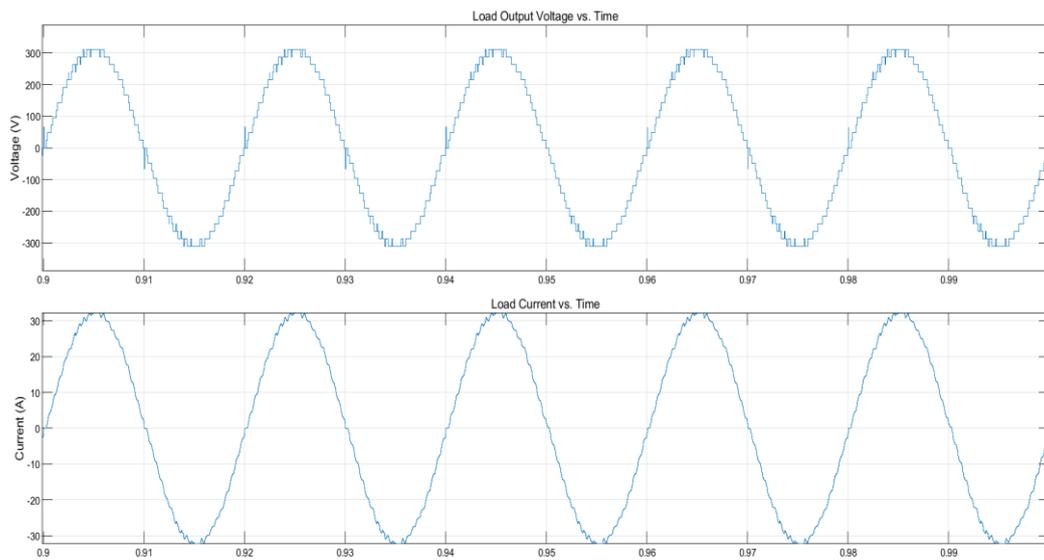
Figure 6-27: 27L-V$_{inv}$, and I$_L$ waveforms

After analyzing the output voltage and current waveforms of MAC27-β$_3$. THD of output voltage (THDv) is 4.65%, and THD of output current (THDi) is 2.26%, as shown in Figure 6-28.
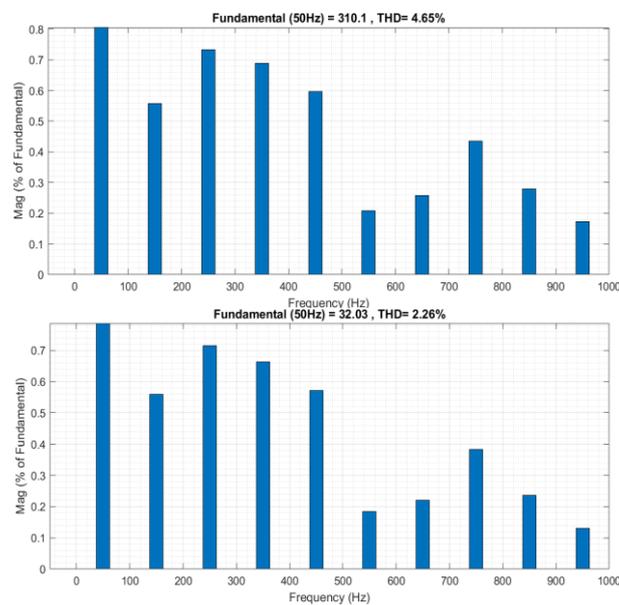
Figure 6-28: Simulink FFT Analysis of V$_{inv}$ and I$_L$, THD (%) for MAC27-β$_3$

6.1.4.2 MAC81-2β_3

Figure 6-29 shows the Simulink model of MAC81-2β_3 in Standalone case. In this case the inverter is feeding an inductive load, this form has the same scheme of MAC81-2β_3.
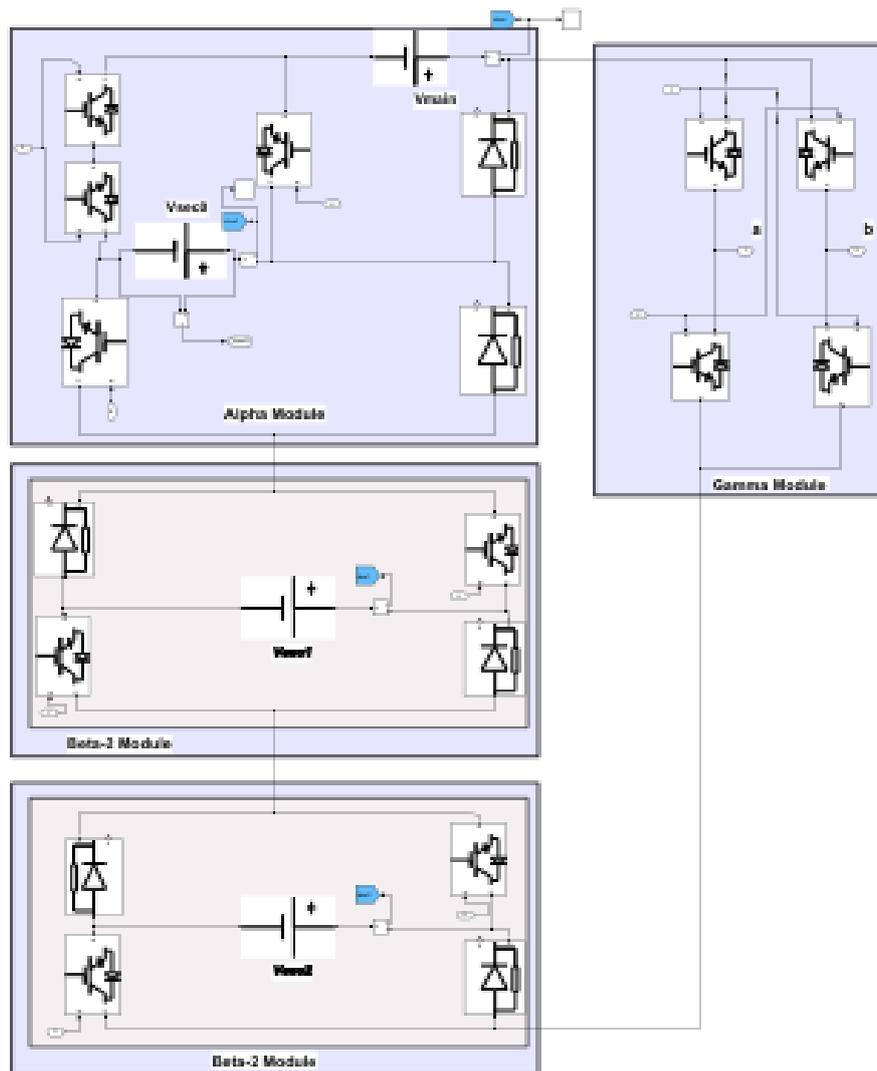
Figure 6-29: MAC81-2β_3 MATLAB Model using DC-sources

The parameters of MAC81-2β_3 inverter setup are illustrated in Table 6-9.

Table 6-9: Specifications of Proposed MAC81-2β3 Model with a load

Parameter	Symbol, Unit	Value
MAC81-2β_3		
Alpha Main DC voltage (V_{main})	V_{main}, V	27E
Alpha Secondary DC voltage	V_{sec0}, V	9E
Beta-3 DC voltage	V_{sec1}, V	3E
Beta-3 DC voltage	V_{sec2}, V	E=$\frac{311}{40}$
Number of Levels	N_{level}	81

The LS-SPWM twelve-carriers (V_{cr}) and control signals (V_{cn}) are illustrated in Figure 6-30.
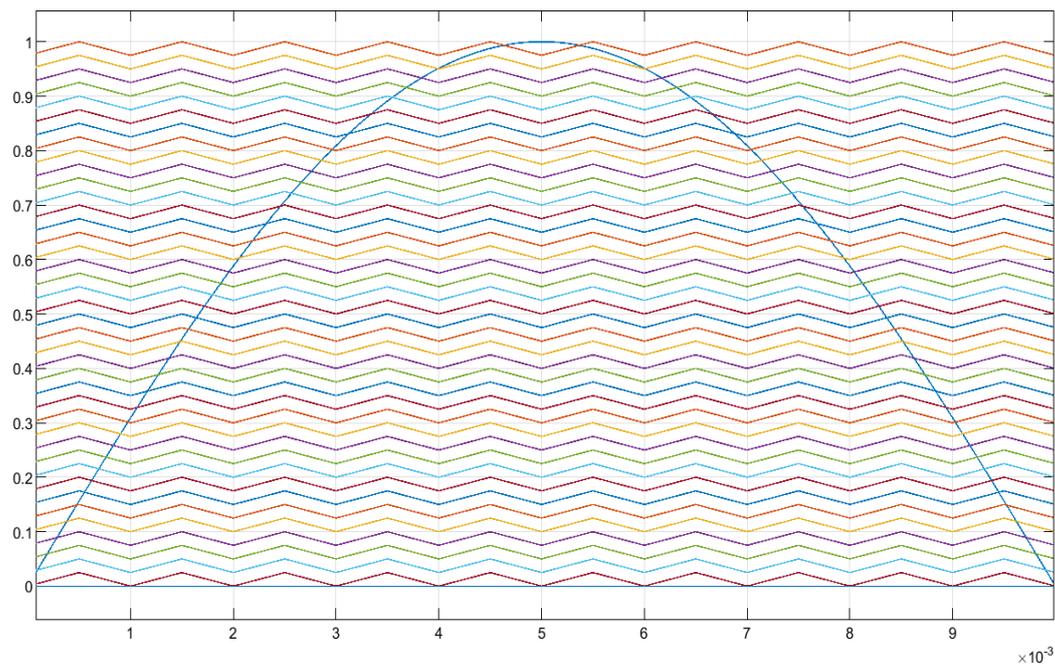
Figure 6-30: LS-SPWM 40-carriers and control signal for positive half-cycle

Output voltage (V_{inv}) with 41-level voltage and semi-sine load current waveform (I_L) are shown in Figure 6-31.
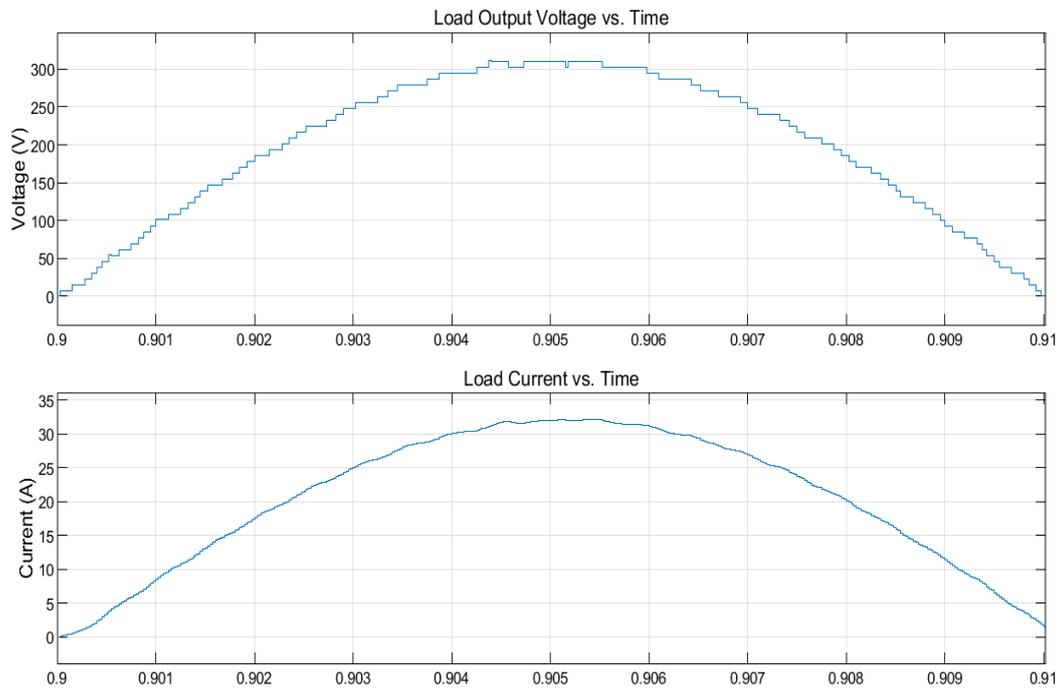
Figure 6-31: Positive half-cycle 81L-V$_{inv}$, and I$_L$ waveforms of MAC81-2β$_3$

6.1.5 MAC49-2α$_c$

Figure 6-32 shows the Simulink model of MAC49-2αc in Standalone case. In this case the inverter is feeding an inductive load, this form has the same scheme of MAC49-2α$_c$.
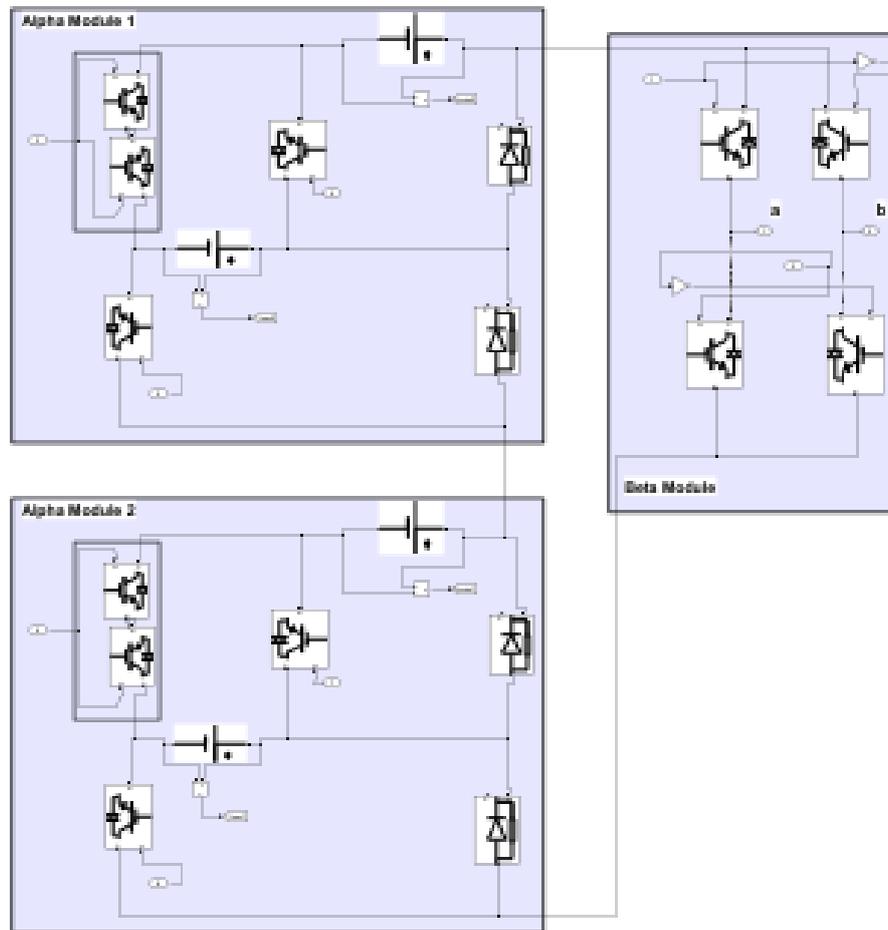
Figure 6-32: MAC49-2α_c MATLAB Model using DC-sources

The parameters of MAC49-2α_c inverter and the load setup are illustrated in Table 6-10.

Table 6-10: Specifications of Proposed MAC49-2α_c Model with a load

Parameter	Symbol, Unit	Value
MAC49-2αc		
First Alpha Main DC voltage	V_{main}, Volts	15E
First Alpha Secondary DC voltage	V_{sec0}, Volts	5E
Second Alpha Main DC voltage	V_{main}, Volts	3E
Second Alpha Secondary DC voltage	V_{sec0}, Volts	$E=\frac{311}{48}$
Number of Levels	N_{level}	49

The LS-SPWM twelve-carriers (V_{cr}) and control signals (V_{cn}) are illustrated in Figure 6-33.
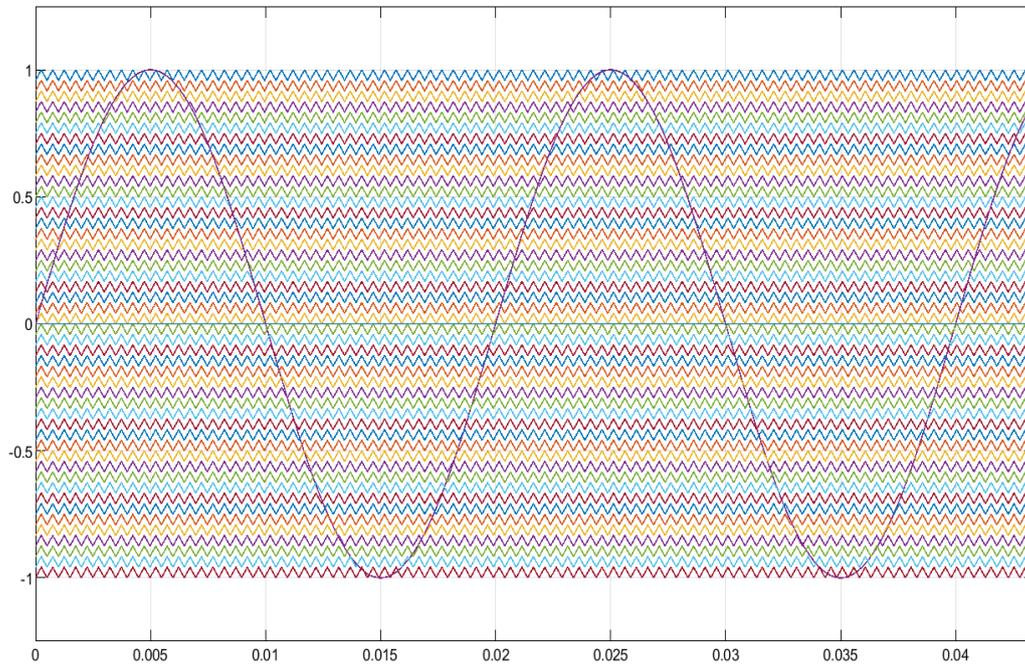
Figure 6-33: LS-SPWM 48-carriers and control signal

Output voltage (V_{inv}) with clear 49-level voltage and semi-sine load current waveform (I_L) are shown in Figure 6-34.
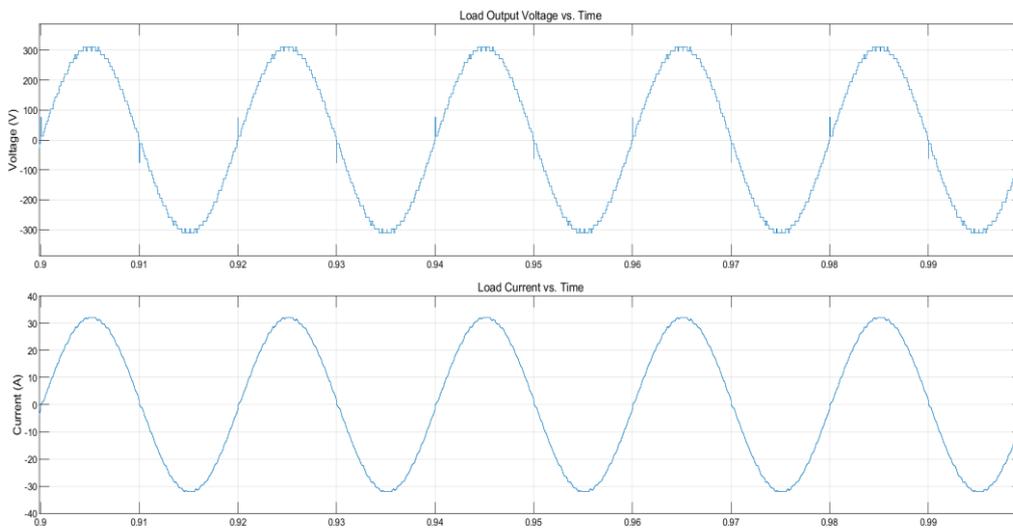
Figure 6-34: 49L-Vinv, and IL waveforms

After analyzing the output voltage and current waveforms. THD of output voltage (THDv) is 2.98%, and THD of output current (THDi) is 1.11%, Figure 6-35.
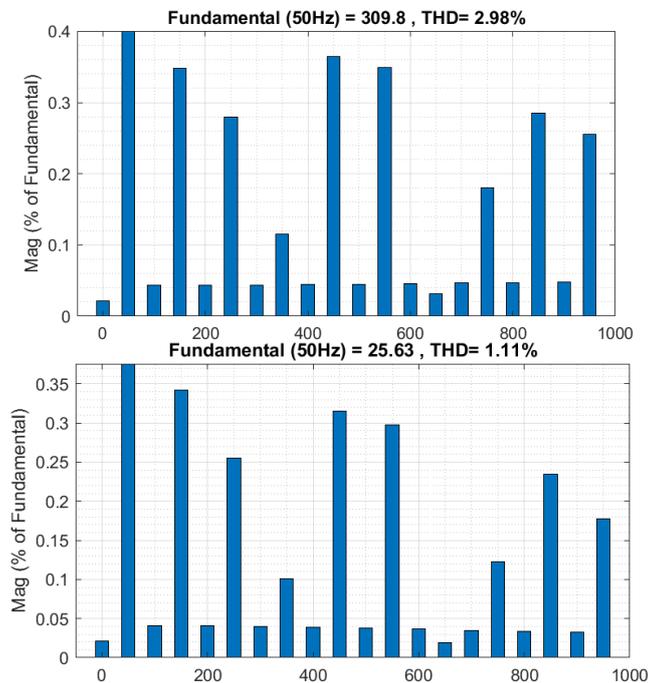
Figure 6-35: Simulink FFT Analysis of V_{inv} and I_L, THD (%) for MAC49-2α_c

6.2 Grid-connected MAC

This simulation is to verify the Grid-connected single DC-source MAC9 (M-DCS), MAC7(1-DCS) and MAC-β_1(1-DCS), The Grid-side model parameters, series R_{grid} and L_{grid} are taken for comparison purpose [48]. Grid MATLAB Model is shown in Figure 6-36, this model is connected to MAC in two nodes (a, b).
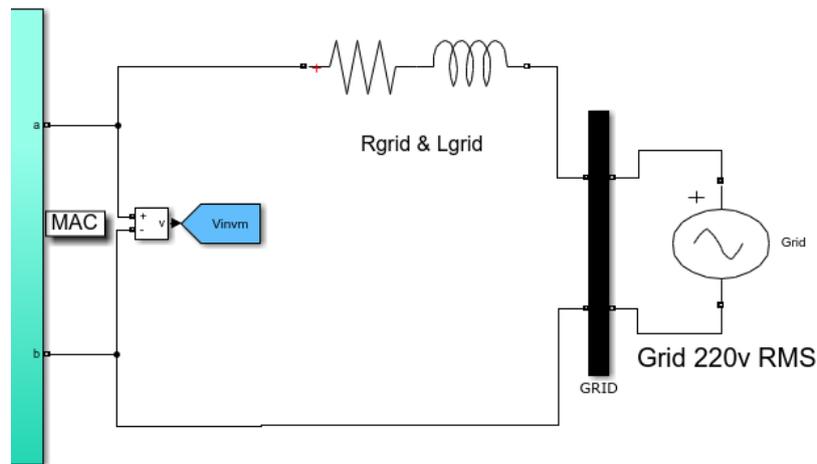
Figure 6-36: Grid MATLAB Configuration

The parameters of Grid model setup are listed in Table 6-11.

Table 6-11: Specifications of Grid-side Configuration

Grid-side Parameter	Symbol, Unit	Value
Grid Voltage (L-N)	$V_{grid, rms}$, Volts	220
Grid AC voltage (peak)	V_{griap}, Volts	311
Frequency	f, Hz	50
Phase Angle	θ, Degree	0
Resistance	R_{grid}, Ω	0.01
Inductance	L_{grid}, mH	2.5

Each proposed form of MAC for this section includes the model setup with output voltage must be greater than grid voltage for desired power flow. The optimal value of critical weighting factor is selected for each form based on

minimum value of THDi, and in the same time the ripple of capacitor voltages is lower than 5%.

6.2.1 MAC9 (M-DCS) for single DC-source

Figure 6-37 shows the Simulink model of MAC9 in grid-connected case, the grid has an inductor of 2.5 mH and a resistor of 0.01 ohm.
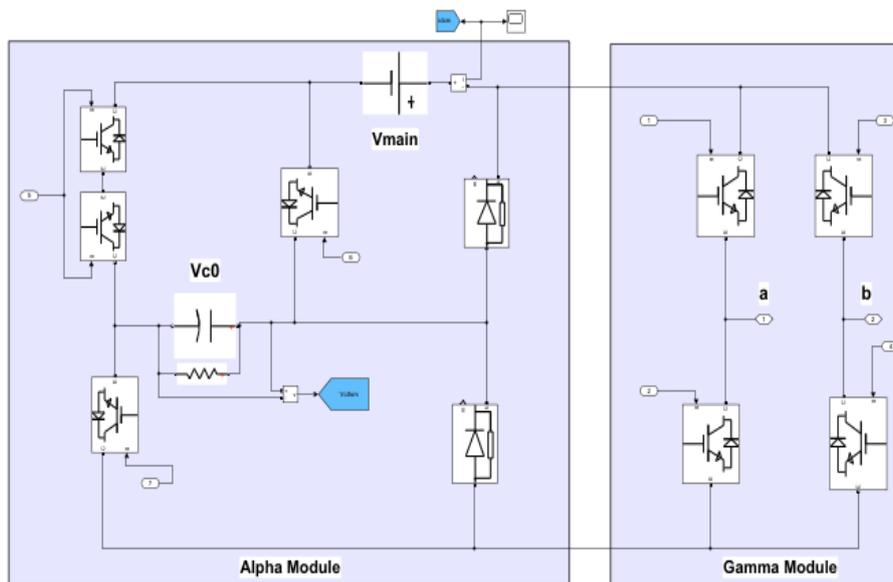
Figure 6-37: MAC9 MATLAB Model using single DC-source

The parameters of MAC9 inverter setup are listed in Table 6-12.

Table 6-12: Specifications of Proposed MAC9 Configuration

MAC9 Parameter	Symbol, Unit	Value
Input DC voltage	V_{main}, V	300
Desired C_0 voltage	V_{C0}, V	E=100
Capacitance of C_0	C_0, mF	3
Sampling Time	Ts, μs	25
Number of Levels	N_{level}	9
Output AC voltage (peak)	V_{inv}, V	400
Weighting Factors	K_g, K_{C0}	1, 3

The nine-level of MAC9, voltage of the capacitor, and grid current are sequentially illustrated in Figure 6-38, also the voltage of capacitors, where they are controlled to be around the reference initial value ($V_{C0} = E = 100V$), and the steady state error is relatively less than 5% (small), by noting these waveforms are achieved in optimum values of weighting factors (K_g & K_{C0}). These factors are estimated based on lowest THD value of output current. Higher value of this factor means higher capacitors voltage errors ($\Delta V_{C0, rms} = 2.19$). 9L-Vinv, V_{C0}, $I_{grid, ref}$, and I_{grid} are illustrated in Figure 6-38.
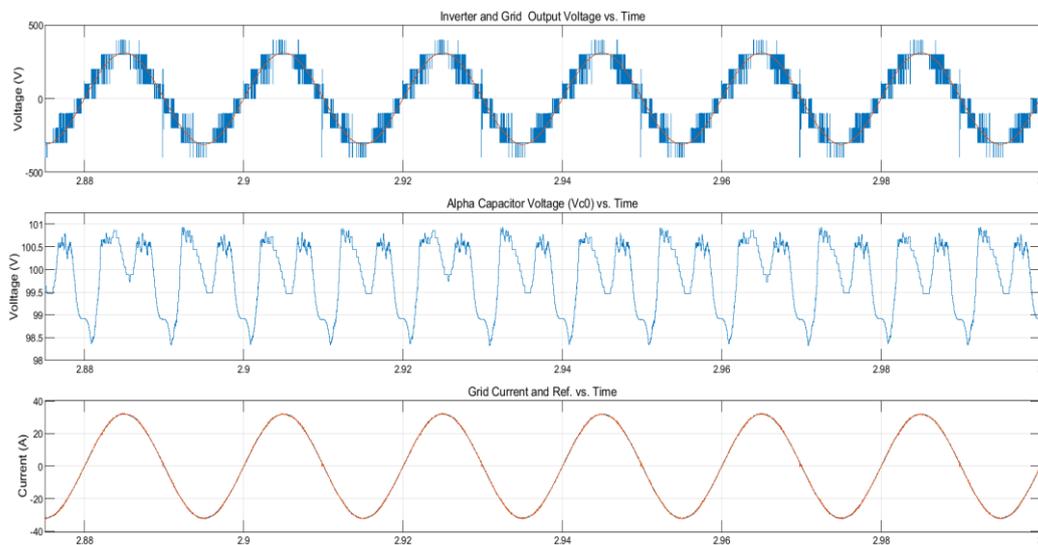
Figure 6-38: 9L-V_{inv}, V_{C0}, V_{C1}, and I_{grid} with I_{grid_ref} waveforms

After analyzing the output current waveform of inverter, I_{grid} is very closed to I_{grid_ref}, RMS error in Igrid is about 0.36, it is very small, $\Delta V_{C0} = 0.75$. THD of output current (THDi) is 1.54%, and THD of output voltage (THDv) is 25.61%, Figure 6-39.
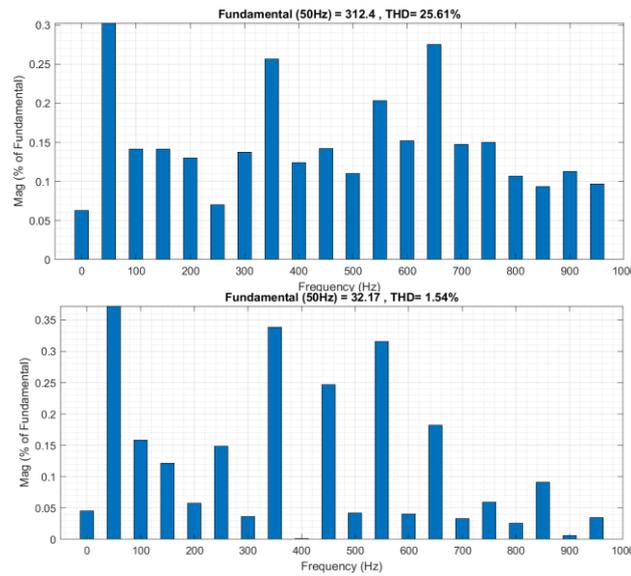
Figure 6-39: Simulink FFT Analysis of I_{grid} and V_{inv}, and THD (%) for MAC9

6.2.2 MAC7 (1-DCS) for single DC-source

Also, Figure 6-37 shows the Simulink model of MAC7 in grid-connected case,

MAC7 and MAC9 are the same circuit with different sources ratios, the grid has an

inductor of 2.5 mH and a resistor of 0.01 ohm.

The parameters of MAC7 inverter setup are listed in Table 6-13.

Table 6-13: Specifications of Proposed MAC7 Configuration

MAC7 Parameter	Symbol, Unit	Value
Input DC voltage	V_{main}, V	266
Desired C_0 voltage	V_{C0}, V	E=133
Capacitance of C_0	C_0, mF	3
Sampling Time	Ts, µs	25
Number of Levels	N_{level}	7
Output AC voltage (peak)	V_{inv}, V	400
Weighting Factors	K_g, K_{C0}	1, 3

The seven-level of MAC7, voltage of the capacitor, and grid current are

sequentially illustrated in Figure 6-40, also the voltage of capacitors, where they

are controlled to be around the reference initial value ($V_{C0} = E = 133V$), and the steady state error is relatively less than 5% (small), by noting these waveforms are achieved in optimum values of weighting factors (K_g & K_{C0}). These factors are estimated based on lowest THD value of output current. Higher value of this factor means higher capacitors voltage errors ($\Delta V_{C0, rms} = 2.17$). 7L-$V_{inv}$, V_{C0}, $I_{grid, ref}$, and I_{grid} are illustrated in Figure 6-40.
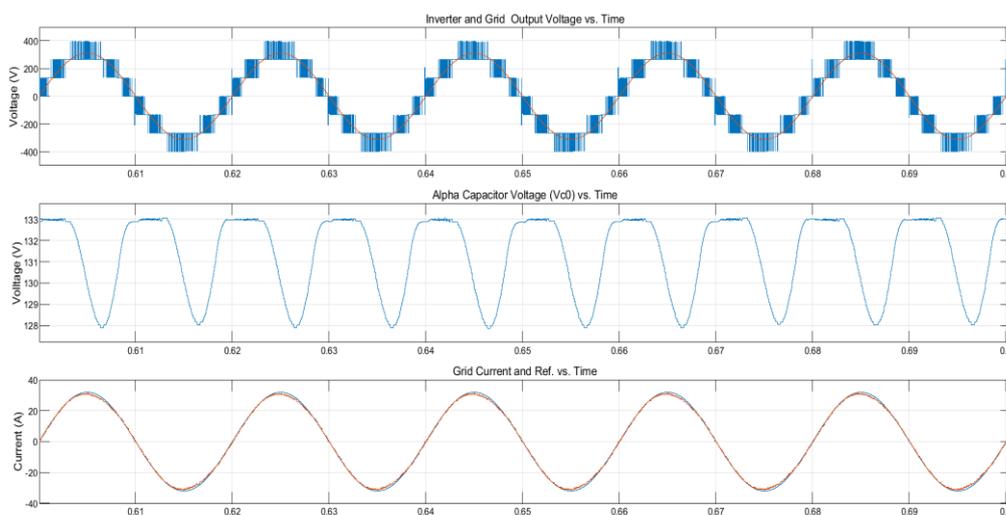
Figure 6-40: 7L-V_{inv}, V_{C0}, V_{C1}, and Igrid with I_{grid_ref} waveforms

After analyzing the output current waveform of inverter, I_{grid} is very close to I_{grid_ref}, RMS error in I_{grid} is about 0.81, it is very small, $\Delta V_{C0} = 2.51$. THD of output current (THDi) is 2.45%, and THD of output voltage (THDv) is 24.83%, Fig 6.41.
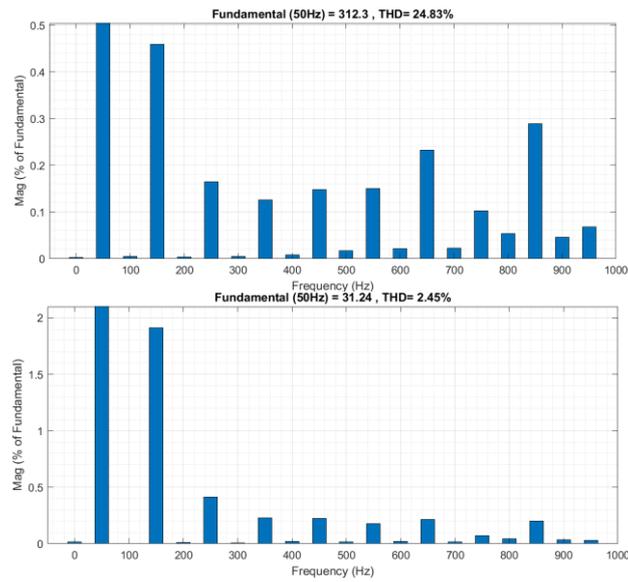
Figure 6-41: Simulink FFT of I_{grid} and V_{inv}, THD (%) for MAC7

6.2.3 MAC11-β_1 (1-DCS)

Figure 6-42 shows the Simulink model of MAC11-β_1 in grid-connected case, the grid has an inductor of 2.5 mH and a resistor of 0.01 ohm.
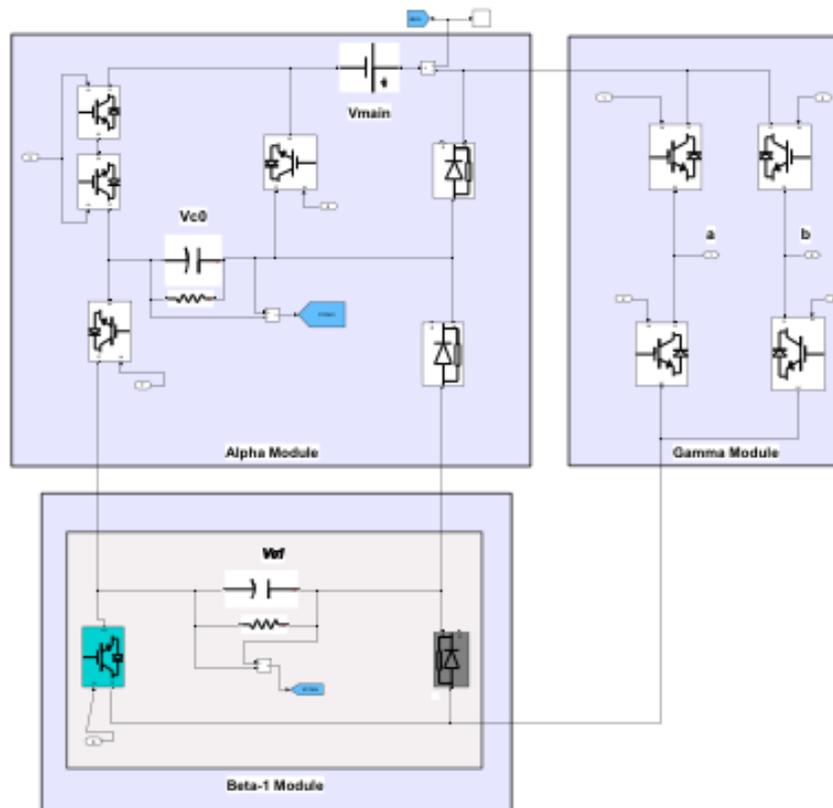
Figure 6-42: MAC11-β₁ MATLAB Configuration

The parameters of MAC11-β₁ inverter setup are listed in Table 6-14.

Table 6-14: Specifications of Proposed MAC11-β₁ Configuration

MAC11-B1 Parameter	Symbol, Unit	Value
Desired Output voltage of inverter	V_{inv}, Volts	360
Input DC voltage	V_{main}, Volts	288
Desired C_0 voltage	V_{C0}, Volts	144
Desired C_1 voltage	V_{C1}, Volts	E=72
Capacitance of C_0	C_0, mF	6
Capacitance of C_1	C_1, mF	1
Sampling Time	T_s, μs	25
Number of Levels	N_{level}	11
Output AC voltage (peak)	V_{inv}, Volts	360
Weighting Factors	K_g, K_{C0}, and K_{C1}	1, 3, and 7

The eleven-level of MAC11-β_1, voltage of the capacitors, and grid current are sequentially illustrated in Figure 6-44, also the voltage of capacitors, where they are controlled to be around the reference initial values ($V_{C0} = E = 72$ and $V_{C1} = 2E = 144$), and the steady state error is relatively less than 5% (small), by noting these waveforms are achieved in optimum values of weighting factors (K_g, K_{C0}, and K_{C1}).

K_g, K_{C0}, and K_{C1} are estimated based on lowest THD value of output current. Higher value of this factor means higher capacitors voltage errors ($\Delta V_{C0, rms} = 0.36$ and $\Delta V_{C1, rms} = 0.07$). 11L-$V_{inv}$, V_{C0}, V_{C1}, $I_{grid, ref}$, and I_{grid} are illustrated in Figure 6-43,
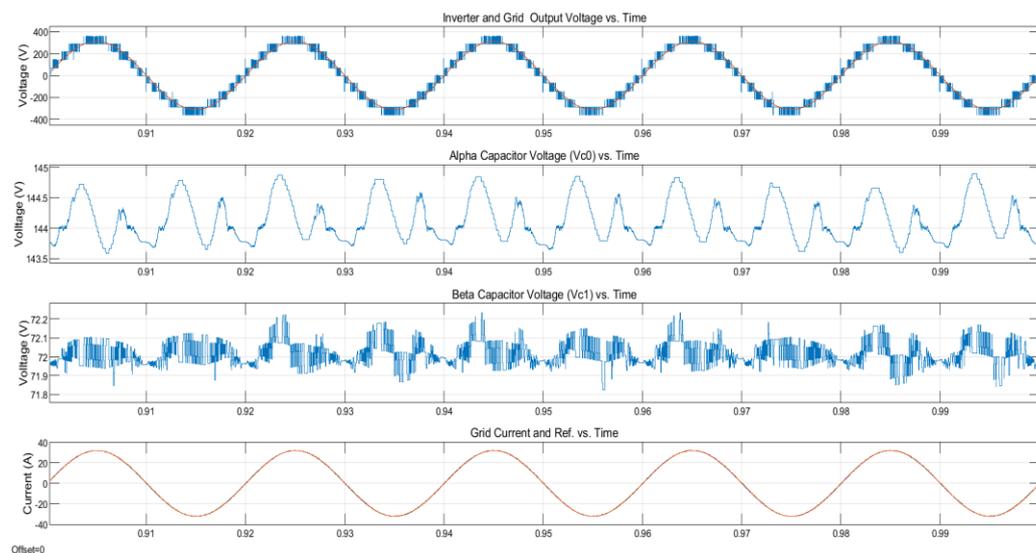
Figure 6-43: 11L-V_{inv}, V_{C0}, V_{C1}, and I_{grid} with I_{grid_ref} waveforms for MAC11-β_1

After analyzing the output current waveform of inverter, I_{grid} is very close to I_{grid_ref}, RMS error in I_{grid} is about 0.26, it is very small. THD of output current (THDi) is 0.89%, and THD of output voltage (THDv) is 14.45%, Figure 6-44.
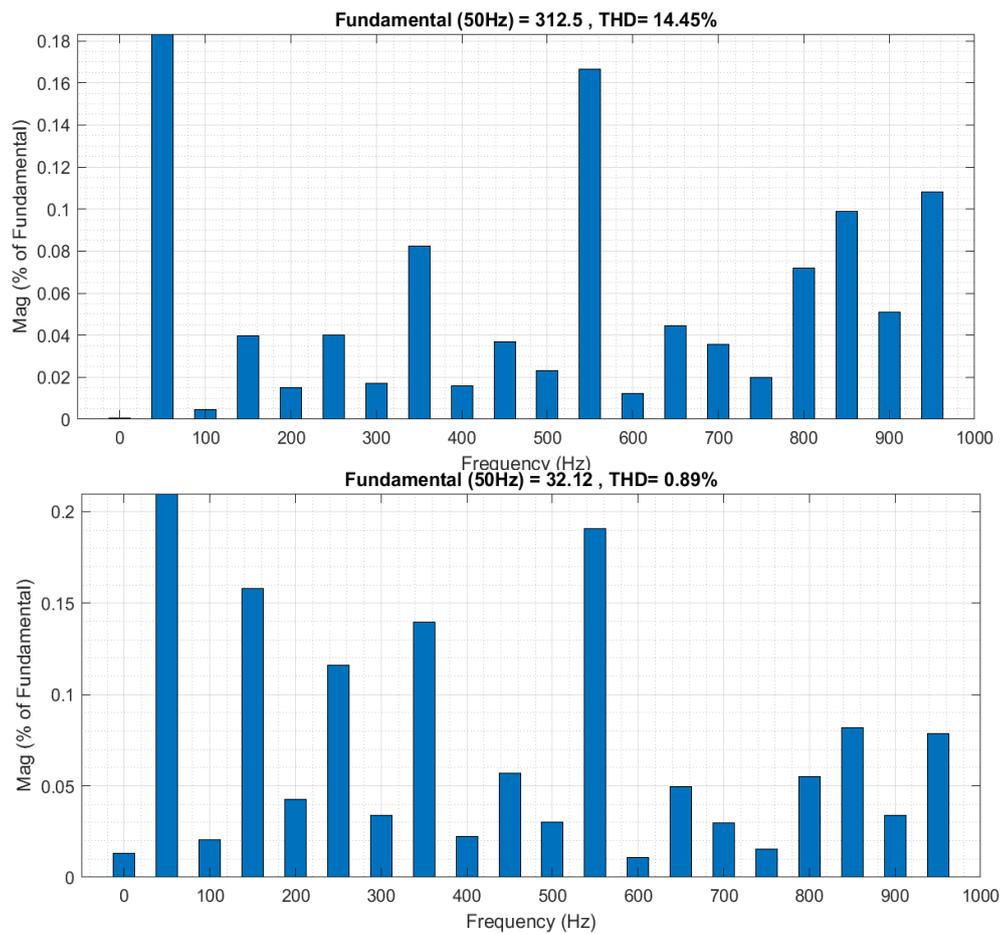
Figure 6-44: Simulink FFT of V_{inv} and I_{grid}, THD (%) for MAC11-β_1

6.2.4 MAC11-β1 vs. PUC9 Comparison

The comparison between two eight-switches topologies based on the same controller, sources ratio, and grid setup as illustrated in Table 6-15.

The proposed topology requires 8 switches with 3 diodes generates 11 voltage levels, THDi is the lowest (0.89%)

Table 6-15: Comparison between MAC11-β1 (1-DCS) vs. PUC9 (1-DCS)

Grid-connected	N_{SW}	N_S	N_C	N_D	N_L	THDi (%)
PUC9 (1-DCS)	8	1	1	0	9	1.13
The proposed MAC11-β_1 (1-DCS)	8	1	1	3	11	0.89

6.3 Changings Scenarios Effects On MAC11-β_1 Grid-Connected

In this section, three test scenarios are analyzed of Grid-connected MAC11-β_1 configuration; first one includes the change of Grid voltage (step change with ±10% of V_{grid}), second, the change of Grid current, and the last one is change of connected inductive load in two values.

6.3.1 Grid Voltage Change Scenario

This scenario based on two voltages of grid, case 1: Sag which Grid voltage is 90% of rated voltage, and after that case 2: swell with increasing to 10% over rated voltage; all is done as a step for each one. Rated voltage with Sag and Swell events is shown in one signal for illustration, Sag starts at t=0.1 sec and the Swell at t=0.2 sec, Figure 6-45.
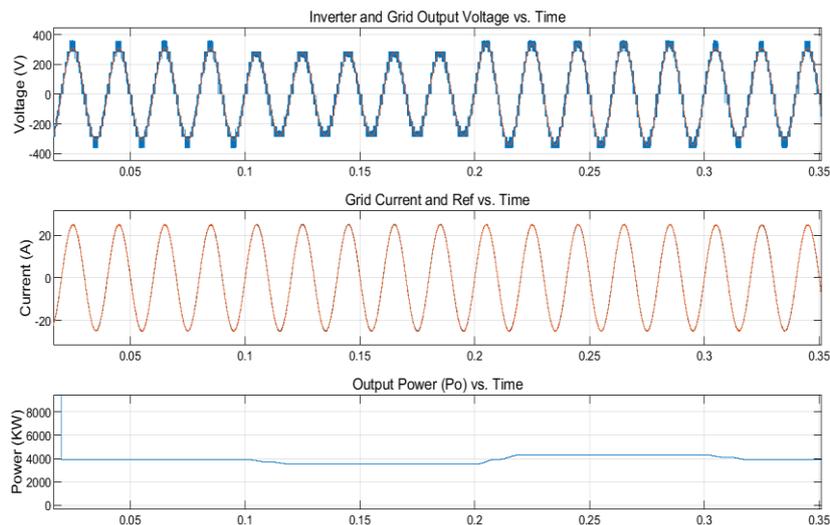
Figure 6-45: V_{inv} with V_{grid_ref}, Igrid, and P_o waveforms with Sag and Swell events

The slight change in THDi and THDv of grid current and voltage, respectively (change < 0.05%), and in ΔV_{C0} and ΔV_{C1} is still within the acceptable range.

6.3.2 Grid Current Change Scenario

Transient response of the proposed inverter when the Grid current is changed is the purpose of this scenario, for this test; the grid current is assumed that's changed as a step from 9.09A to 18.18A, the response of this Extended-MAC is appeared very quick as illustrated in Figure 6-46. the ripples of V_{C0} and V_{C1} are increased slightly and still small. The output power of the inverter is changed from 2KW to 4KW in one cycle incrementally.

The last scenario of changed I_{grid} is done at t=0.1043.
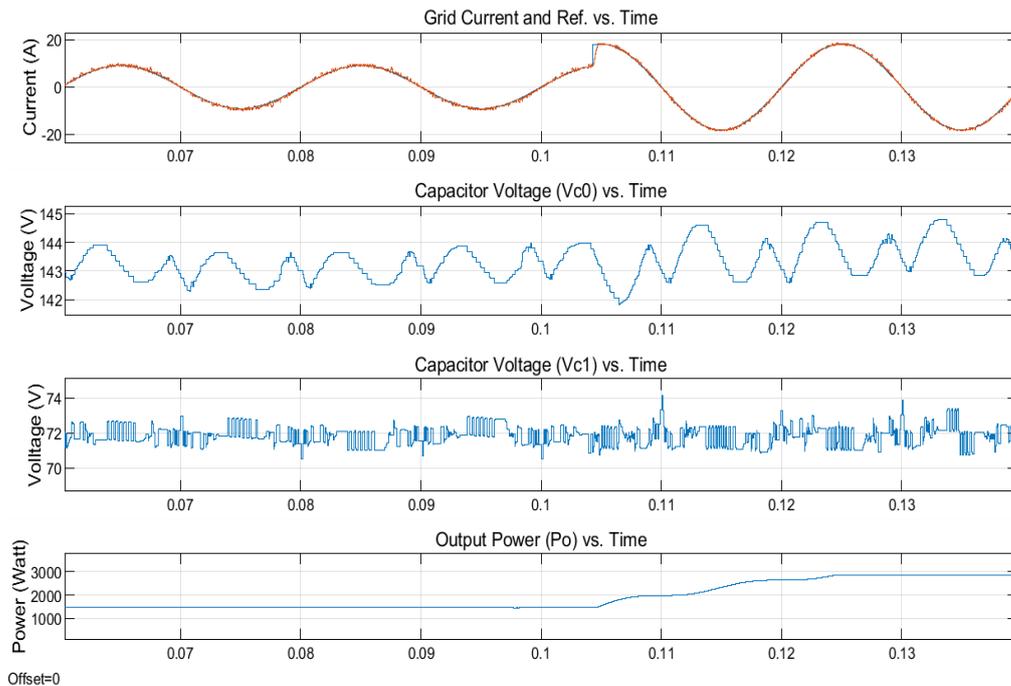
Figure 6-46: Waveforms of I_{grid_ref}, Igrid, V_{C0}, V_{C1}, and P_o during step change of I_{grid_ref}

RMS error in Igrid is about 0.37 after the change, and it's very small. Figure 6-47 shows the V_{inv} of the inverter and I_{grid} during step change of grid current

reference; Vinv is still the same without any change, but the grid current has slight increasing in RMS error.
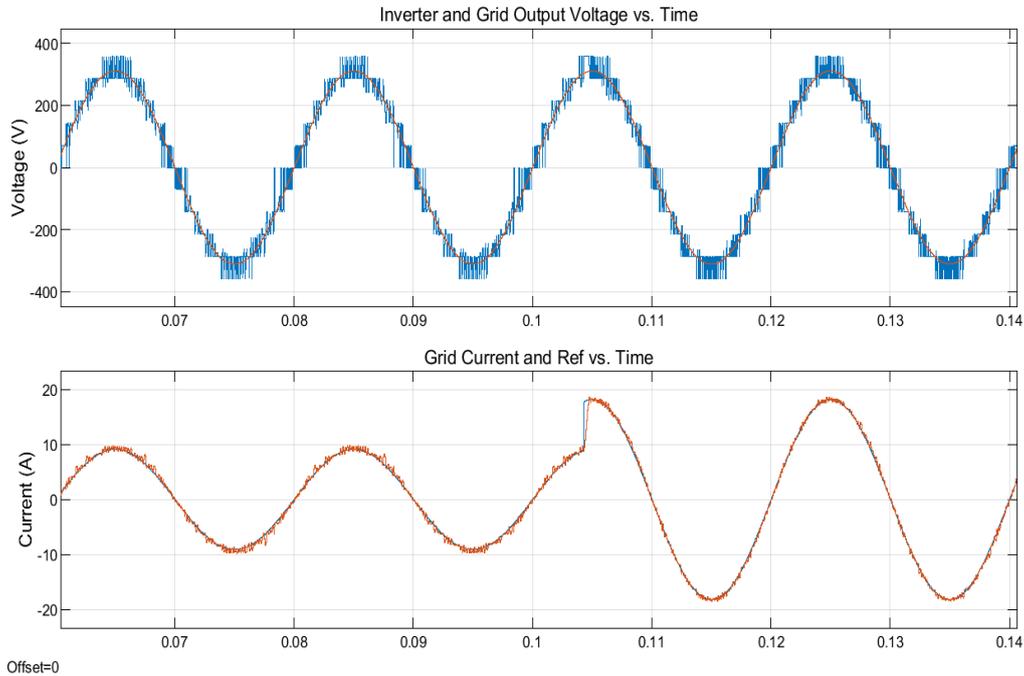
Figure 6-47: V_{inv} of the inverter and I_{grid} with I_{grid_ref} waveforms during step change of grid current reference

6.3.3 Adding Loads Scenario on Single DC-source MAC9 (M-DCS)

The last scenario is the response of single DC-source MAC9/Grid-connected (M-DCS configuration) when adding the load, the simple first order filter of R_f and L_f is used, the proposed FCS-MPC is applied with small RL-filter with R_f and L_f instead of R_{grid} and L_{grid}, and the objective current is I_{inv} instead of I_{grid}, the node CP is the output node of the filter, Figure 6-48. For this test; three different loads

(RL-Load) values are used. The values for R_f and L_f are 0.1 Ω and 2.5 mH, respectively, these values are used from [53] for the proposed system frequencies.
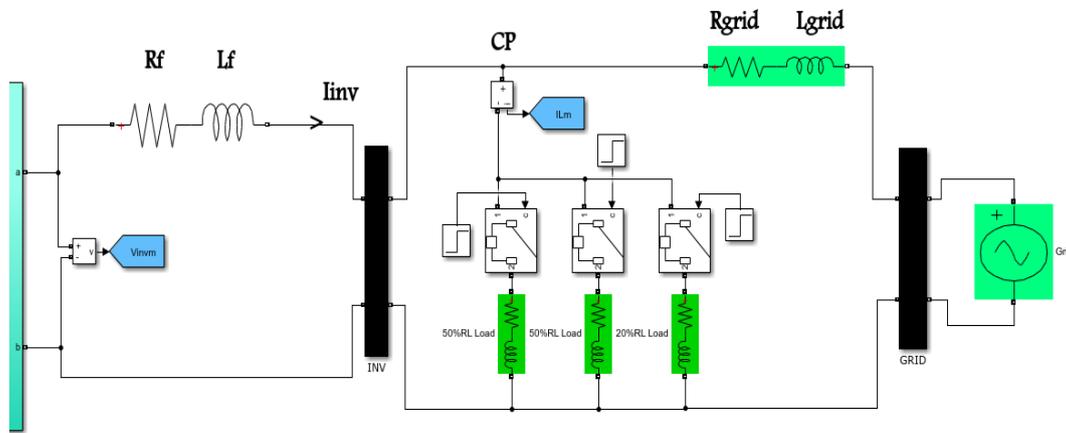
Figure 6-48: MATLAB Model of Single DC-source MAC9 with a load in Grid-connected

The load is selected of DPF=0.999, and the rated output power of the proposed inverter is to be 5KVA, the simulation parameters for this section are listed in Table 6-16.

Table 6-16: Load Matlab Model Parameters (MAC9\Grid-connected)

Parameter	Symbol, Unit	Value
Rated Apparent Power Inverter	S_I, KVA	5
Reference current	I_{ref}, A	32.12
Load		
Displacement Power Factor	DPF	0.999
Full Apparent Power Load	S_L, KVA	5
Full Real Power Load	P_L, KVAr	4.995
Full Reactive Power Load	Q_L, KVAr	0.2
Filter [53]		
Resistor	R_f, Ω	0.1

Inductor	L_f, mH	2.5

The first load is 50% of desired load and the other is a full load, then 120% of full load, the load is switched from no-load to first at t=0.5 sec, from first load to second one at t=1.0, and for last case at t=1.5.

I_L during step change of cases: 50% of Load, Full-Load, and 120% of load. The current of load is increasing during last mentioned cases based on value of the load, in addition of grid connection with 220 Vrms and 32.12 A peak reference current, the current of grid is injected to grid in the first case and feeds the load in third one, and no-value to load or grid injection in second case, Figure 6-49. When the load reach 120% of the full value, the grid current is inversed to feed the load.
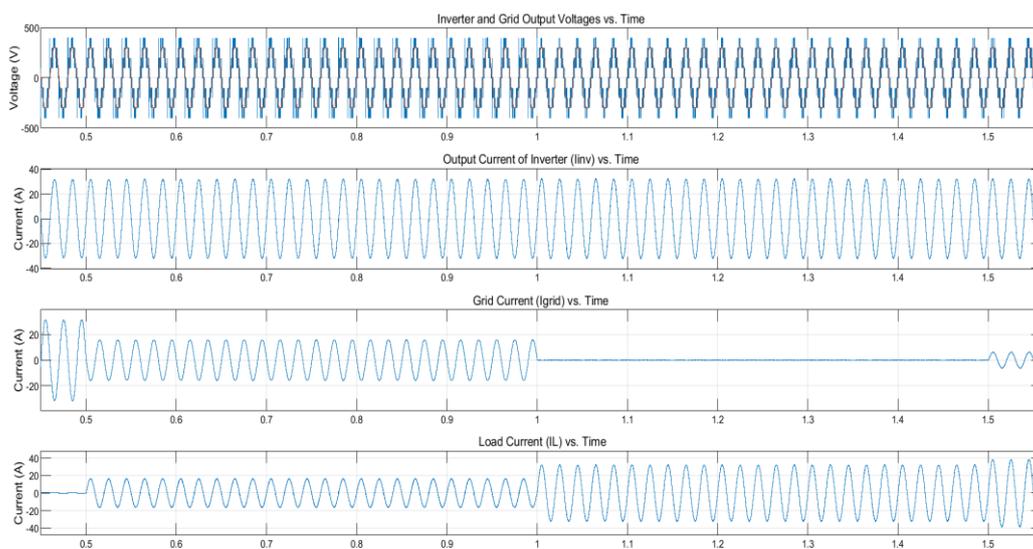
Figure 6-49: V_{inv} and I_{inv} of the inverter, I_{grid}, I_L waveforms during step change of cases:

No-Load, 50% of Load, Full-Load, and 120% of Load.

By noting the voltage spikes on output voltage signal in time interval before the resistive Load is connected to the proposed system, Figure 6-50.
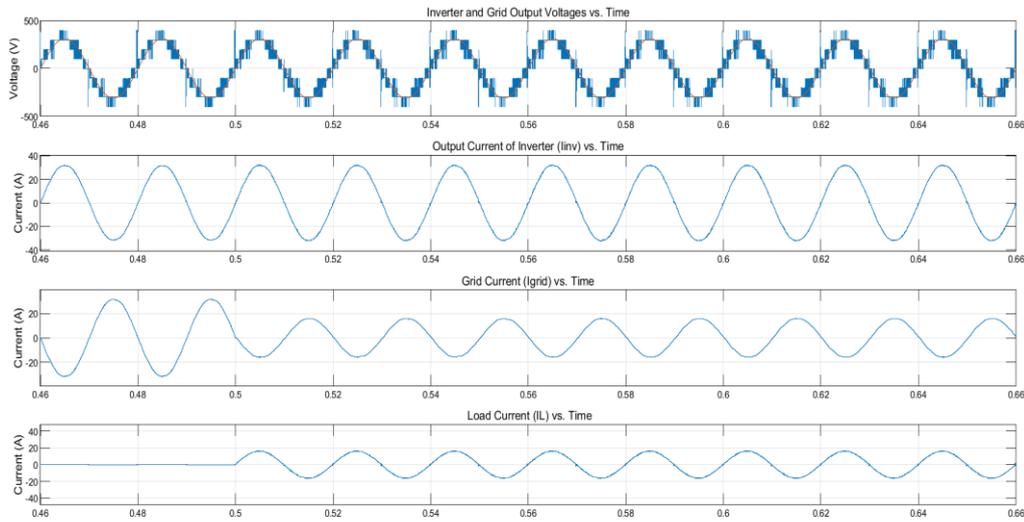
Figure 6-50: Zoom-in V_{inv} with spikes and I_{inv}, I_{grid}, I_L during step change of cases

Voltage spikes issue appears in topologies that are based on switched-capacitor with diode topologies or their states include active diode in inductive load case due to unidirectional power flow, this voltage spikes issue is minimized by connecting an LC-filter cross the load [54]. Figure 6-51 shows P_{in}, P_L, P_{grid} waveforms during step change of cases: No-Load, 50% of Load, Full-Load, and 120% of Load by noting the input power divide to load and grid.
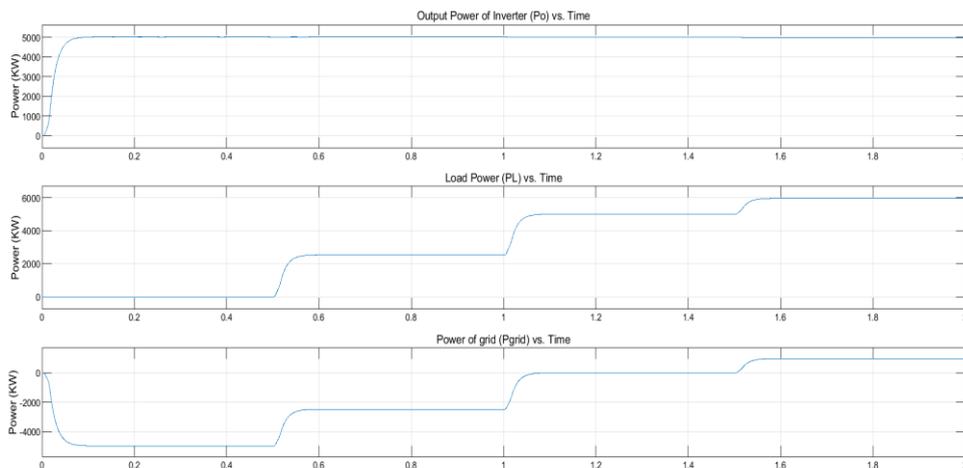
Figure 6-51: P_O, P_L, P_{grid} during step change of cases: No-Load, 50% of Load, , Full-Load, and 120% of Load.

6.4   Single DC-source MAC9 (M-DCS) in standalone

The last scenario is the response of single DC-source MAC9 (M-DCS)/standalone with load in closed-loop control, the simple first order filter of R_f and L_f is used, the proposed FCS-MPC is applied with the same frequency setup filters R_f and L_f in [53] instead of R_{grid} and L_{grid}, and the objective current is I_{inv} instead of I_{grid}, the V_{grid} input of FCS-MPC is a sine wave reference of 311V peak ($V_{o,ref}$) instead of grid voltage based on equation (5-19), this method is presented in [55]. The predictive value of output inversion current is found by the following equation:

$$I_o{}^{k+1} = (1 - \frac{R_f * T_s}{L_f}) \, I_{grid}{}^k + \frac{T_s}{L_f} \, .(V_{inv}{}^k - V_{o,ref}) \tag{6-1}$$

MAC9's standalone connection is shown in Figure 6-52.
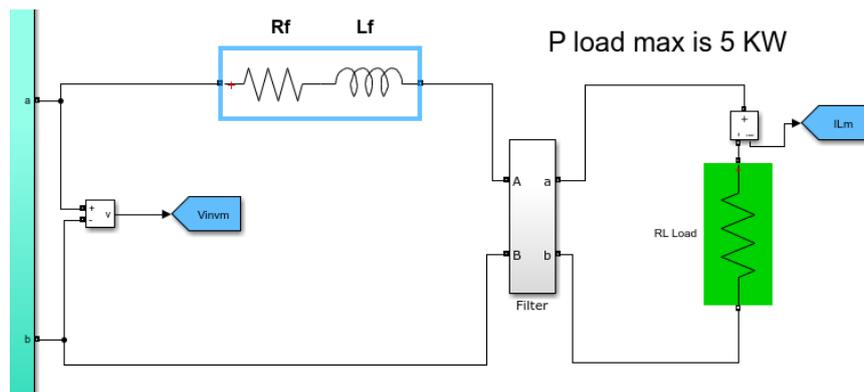
Figure 6-52: MATLAB Model of MAC9's standalone connection

The load is selected of DPF is unity, and the rated output apparent power of the proposed inverter is to be 5 KVA, with a small RL-filter, the simulation parameters for this section are listed in Table 6-17.

Table 6-17: Load Matlab Model Parameters (MAC9(M-DCS) \standalone)

Parameter	Symbol, Unit	Value
Single DC-source MAC9 (M-DCS)		
Rated Apparent Power of inverter	S_I, KVA	5
Reference current	I_{ref}, A	32.12
Reference voltage	V_{ref}, V	311
Load		
Displacement Power Factor	DPF	1
Full Real Power Load	P_L, KW	5
Filter [53]		
Resistor	R_f, Ω	0.1
Inductor	L_f, mH	2.5

The nine-level voltage of single DC-source MAC9 (M-DCS) in standalone connection, the voltage of the capacitor, and load current are sequentially illustrated in Figure 6-53, also the voltage of capacitors, where they are controlled to be around the initial reference value ($V_{C0} = E = 100$), and the steady state error is relatively less than 5% (small). by noting these waveforms are achieved in optimum value of weighting factors (K_g & K_{C0}).

The optimum values of these factors are estimated based on lowest THD value of output current. Higher value of this factor means higher capacitor voltage errors (ΔV_{C0}), K_g & K_{C0} are selected to 1 & 3, respectively.

The error of alpha capacitor (ΔV_{C0}) is less 1 Vrms. V_{inv}, V_{C0}, load voltage (V_o), and current (I_L) are illustrated in Figure 6-53.
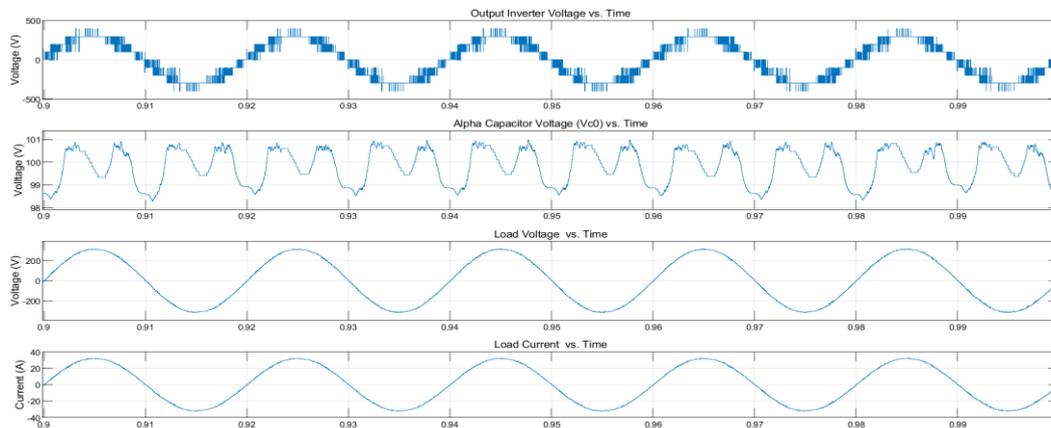
Figure 6-53: V_{inv}, V_{C0}, V_o and I_L waveforms of single DC-source MAC9 (M-DCS) in standalone connection

After analyzing the output current waveform of inverter, I_L is very close to I_{ref}. The output power of single DC-source MAC9 (M-DCS) with a resistive load is 5.00 KW. THD of output voltage (THDv) is 1.39%, THD of load current (THDi) is 1.37% in steady-state, Figure 6-54.
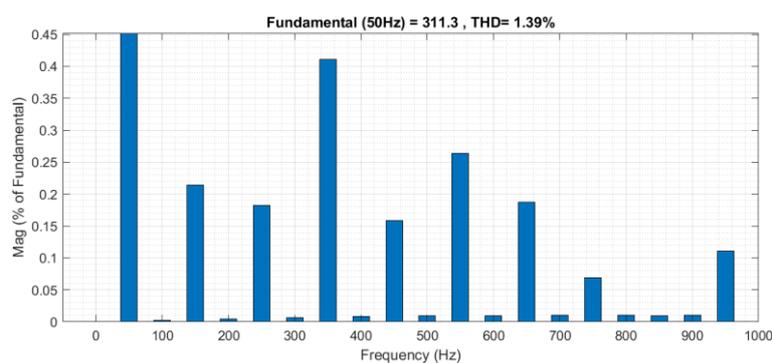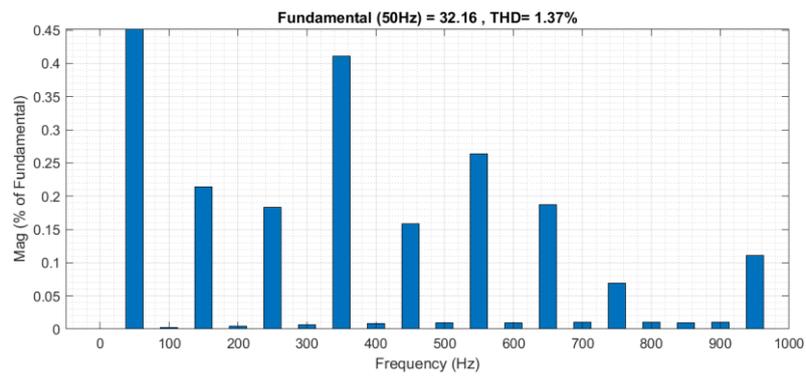
Figure 6-54: Simulink FFT (THD%) of V_o (top) and I_L (bottom) for MAC9 (M-DCS)

The next chapter is the last one, it explains the thesis findings which are the simulation of validation result, features, advantages, and disadvantages of the proposed MAC multilevel inverter. The conclusion and future works at the end.

CHAPTER 7
DISCUSSION & CONCLUSION

In this chapter, the simulation results and features of each MAC form are discussed, then the conclusion of results, and future works.

7.1 Discussion

The simulation results give successful validation of all proposed forms of hybrid MAC by proposed control methods for two source configurations (single/multiple DC-sources). The proposed hybrid MAC topology is the intersection structure of the popular conventional topologies (CHB, FC, and NPC), so it gathers the features of these topologies, MAC has an H-bridge module that gives the modularity of its switch controlling, it can work with a single DC-source likes FC, and it uses diodes to reduce switches counts and to simplify the control method likes NPC, Figure 7-1. Also, Figure 7-1 shows that PUC, CSD, and SC are structures based on only two conventional topologies, for example PUC is consisting of CHB and FC structures.

 The structural benefits of the MAC topology and its essential role in increasing the number of desired voltage-levels of the staircase signal that approximates the sinusoidal waveform, MAC has other important features and applications.

Among these are scalable, different voltage-references ratio operations and single/multiple DC-source configurations, and it is the voltage boosting capability that means minimum main DC voltage source for same desired output AC voltage source.
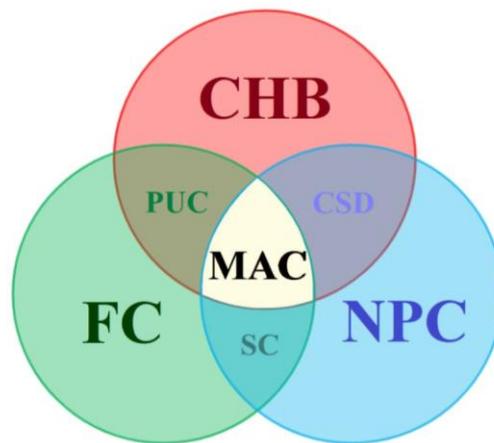
Figure 7-1: MAC verses other topologies based on components type and structure

 MAC in extended form require minimum switches and sources count for each added cell such as single switch in beta-1 module verse the minimum switches count with single source in each cell. Moreover, three Beta cells give several features such as more levels and higher boosting gain with possible lower switches count, also Extended-MAC has other compatible added cell Beta-3.

 In M-DCS, Beta-2 gives higher boosting gain of the proposed added cells, and Beta-3 gives more voltage levels vs. other Beta types, but it requires two switches,

two diodes, and still generate maximum levels verse other competitors with the same number of switches.

MAC gives lower THD of output voltage and current waveforms vs. switches count in each added cell in low switching frequency (f_{SW} =2050 Hz). Table 7-1 shows indicators of performance in standalone mode: the switches count, number of levels, THDv, and THDi in each added cell form of MAC with multiple DC-source in Standalone case. THD reduces by increasing the output voltage levels number. Also, most of THDv are around or below 5% (regarding to IEEE standard 519 which is less 5% [38]), for MAC forms that has THDv over 5%, a filter can be used to reduce these THDv values. When comparison based on levels and components count for the same DC-sources number, MAC21-β_1 (M-DCS) gives 21-levels and requires three DC-sources, eight switches, and three diodes. On other hand, IPUC17 gives 17-levels and requires three DC-sources, and ten switches [56].

Table 7-1: Indicators of Standalone MAC (M-DCS) Performance

		N_{sw}	N_D	Ns	N_L	N_{Cell} (added α or β)	THDv %	THDi %
MAC	Multiple DC-sources				STANDALONE			
- MAC9		7	2	2	9	Basic form	13.72	5.91
-	-	- $xMAC$-β_1						
MAC13-β_1(1-DCS ratio)		8	3	3	13	Single β_1	9.52	4.08
MAC21-β_1		8	3	3	21	Single β_1	5.54	2.65
MAC45-2β_1		9	4	4	45	Double β_1	2.88	1.20
-	-	- $xMAC$-β_2						
MAC23-β_2		9	3	3	23	Single β_2	5.13	2.63
MAC53-2β_2		11	4	4	53	Double β_2	2.89	1.14
-	-	- $xMAC$-β_3						
MAC27-β_3		9	4	3	27	Single β_3	4.65	2.26

-	-		-	*xMAC- α*			
-	MAC49-2α$_c$	10	4	4	49	Double cascaded α	2.93	1.15

In addition to low ripple of capacitors voltage, tracked grid current waveform for single DC-source form, and THD are satisfied the minimum requirements for the major purpose which is a converter with reduced components count for two standalone/grid connection cases. FCS-MPC strategy has estimated parameters which include optimal value of weighting factors, these factors have critical effects on mentioned indicators, so there are selected for each form based on minimum value of THDi, and in the same time the ripple of capacitor voltages is lower than 5%, lower capacitor ripple means close voltage level to reference and lower THD. The weighting factors: K_g, K_{C0}, and K_{C1} are estimated based on lowest THD value of output current. Higher value of this factor means higher capacitors voltage errors.

Table 7-2 shows indicators of performance in each added cell form of single DC-source MAC for Grid-connected and standalone cases. THDi is very small based on Grid parameters (R & L) without any filter, so it could be reduced this more using small filter size. Also, the performance of single DC-source MAC9 (M-DCS) indicates low THDi of load voltage and current, especially after the RL-filter.

Table 7-2: Indicators of MAC (1-DCS configuration) Performance in the two modes

	N_{SW}	N_L	THDi %	THDv %
Grid-Connected for single-DC source				
MAC9 (M-DCS)	7	9	1.54	25.61

MAC7 (1-DCS)	7	7	2.45	24.83
MAC11-β_1(1-DCS)	8	11	0.89	14.45
Standalone for single-DC source				
MAC9 (M-DCS)	7	9	1.37	1.39

Basic-MAC can work in the two sources ratio configurations for seven and nine voltage levels in single/ multiple sources. Where single DC-source MAC9 (M-DCS) uses RL-Filter to demonstrate the behavior of its voltage and current outputs based on THD parameters.

For 1-DCS, All Beta types give the same voltage level, but the difference in redundant states for capacitor voltage balancing, Beta-3 has the big number of levels for the same source count. Beta-1 gives constant boost gain for any number of used extra cells, but it is the reduced component count and with higher voltage levels number verse other topology with same number of switches and voltage-references. On other hand PUC requires two switches.

LVR is a worth comparison factor to solve same LSR factor topologies, MAC satisfies high rank of LVR in same LSR cases, the proposed comparison process in chapter 4 is applicable for all MAC forms.

Other example, the seven-level IPUC, this derivative PUC is presented by using more switches to achieve several advantages such as voltage boosting capability and it consists of nine switches, but single DC-source MAC7 (1-DCS) gives seven-level and boosting feature with seven switches. Also, PUC9 requires eight switches for nine-level without boosting capability, but MAC11-β_1 requires eight switches to give eleven-level with voltage boosting.

From Table 7-1 and Table 7-2 shows lower THDv values in standalone and THDi values in Grid-connected with incremental N_L, respectively. So, the increase in number of levels fulfills THD reductions.

By noting, THD of output injected current to grid is very small in all cases (less 5% based on IEEE standard 519 [38]). Also, the small values of THD don't require big LC-filter size, which is one of major features of MAC. Also, DPF is 0.999 or it isn't high inductive load for validation purposes of major MAC power quality analysis, achieving lower THD and small voltage spikes illustrations. The case of high inductive load in practical condition for future works; the approach of added filter will be applied to minimize the voltage spikes and give more improvements on power quality parameters such as THD, this filter is connected cross MAC inverter output (a, b).

7.2 Conclusions

All proposed forms of hybrid MAC were successfully simulated, the features were illustrated, the indicators of performance referred to highly competitive achievements of the proposed converter: Reduced components count, scalability, boosting capability, different asymmetrical ratio configurations, and more features of MAC were presented in this thesis; it gives maximized levels number and minimized sources & switches count in two asymmetric DC-sources ratio configurations and for standalone and Grid-connected connections.

In future, the quality of MAC can be higher using an LC-filter. Also, many extended topics based on MAC could be studied and applied, such as Three-phase MAC inverter, MMC converter based on MAC structure, and MAC Rectifier.

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Appendix

A1. Complete MATLAB model of single DC-source MAC9 (M-DCS)
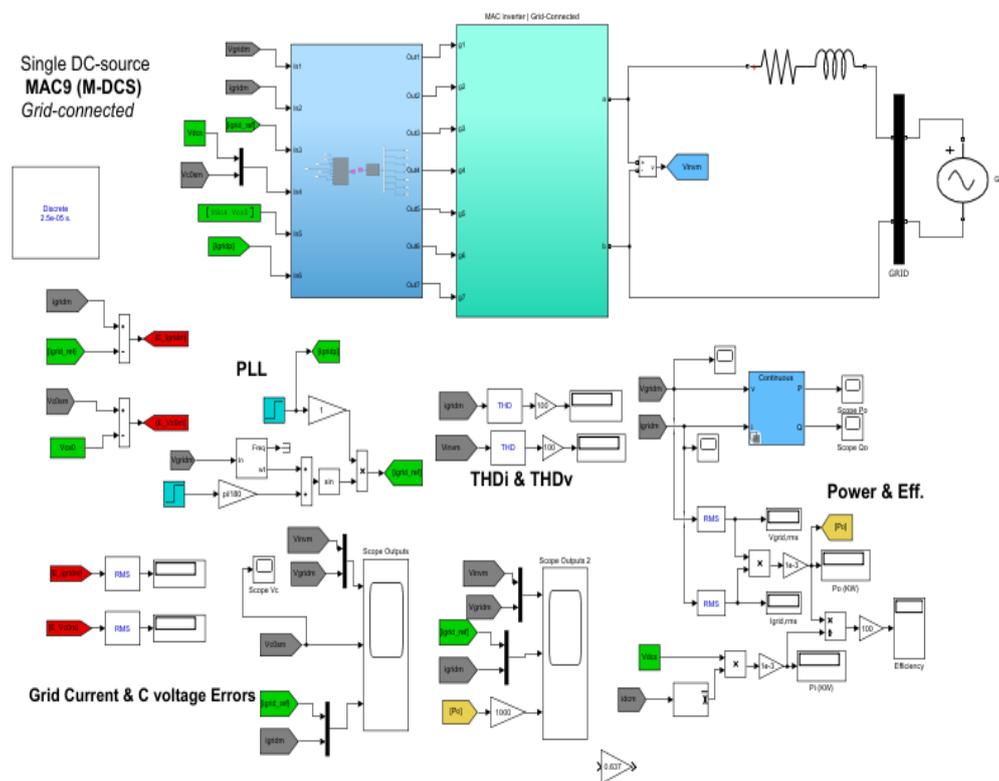
A2. Complete MATLAB model of single DC-source MAC11-β1 (1-DCS) in Grid-connected
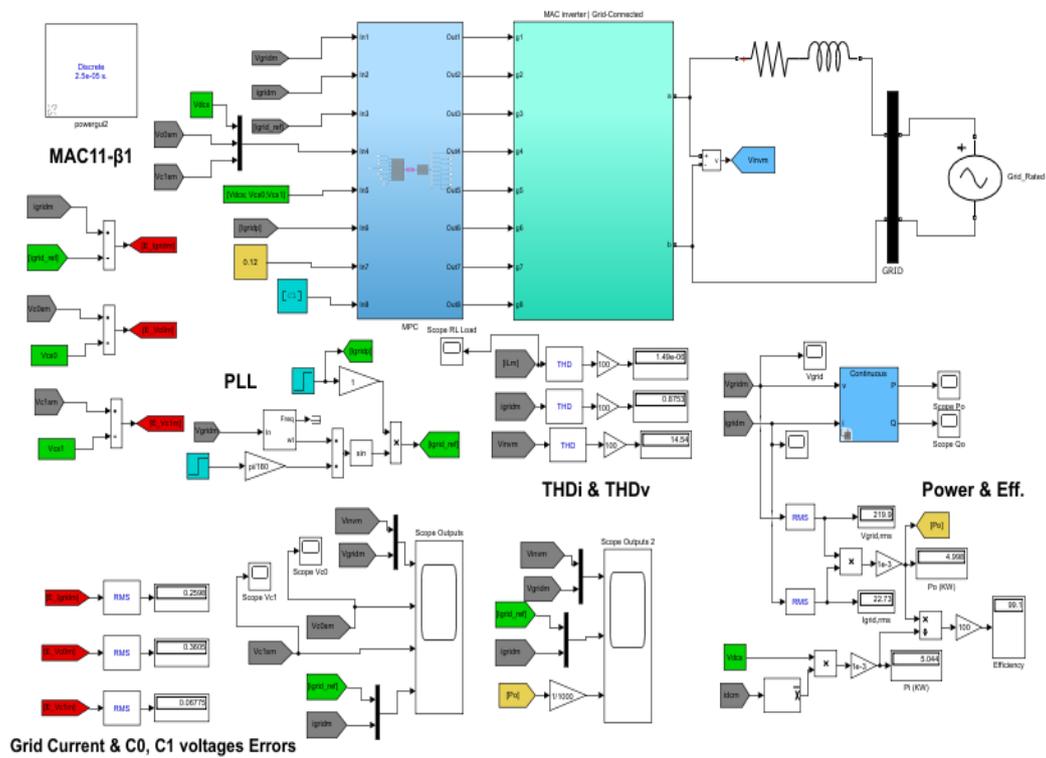
A3. MPC Block
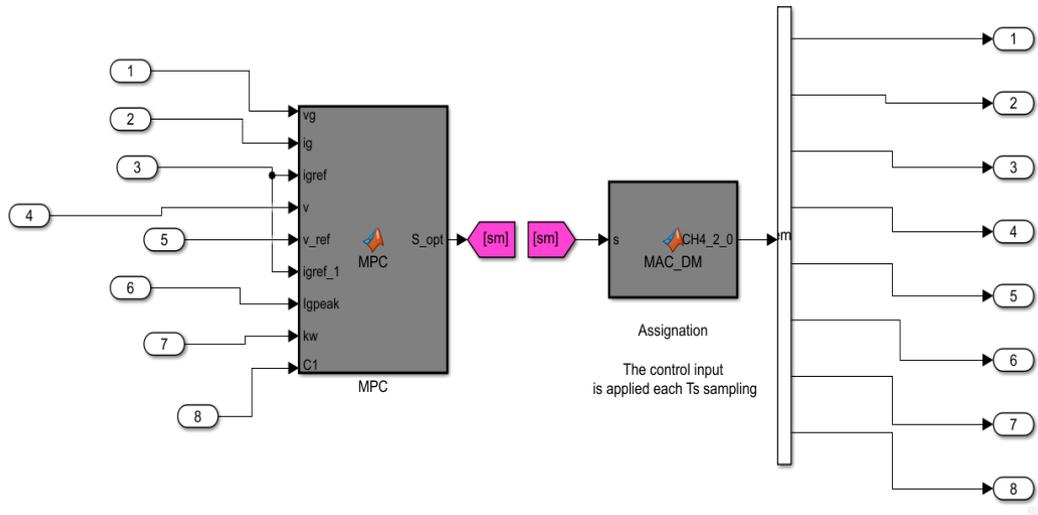
Development of hybrid Multilevel Converters

Modular Added Cell (MAC)

Eng. Majdi Thaher (MSc.)

June 2021